

MANUAL COMPLETO

TTL

INDICE

- CARACTERÍSTICAS DE LOS CIRCUITOS DIGITALES
- ESCALAS DE INTEGRACIÓN DE LOS CIRCUITOS DIGITALES
- SSI, MSI, LSI, VLSI.
- FAMILIAS LOGICAS DE LOS CIRCUITOS DIGITALES
- CARACTERÍSTICAS DE LAS FAMILIAS DIGITALES
- OTROS CIRCUITOS INTEGRADOS TTL
- ABREVIATURAS DE LOS CIRCUITOS DIGITALES
- INDICE SEGÚN LA CARACTERÍSTICAS DE LOS TTL

Características generales de los circuitos digitales

ESCALAS DE INTEGRACION DE LOS CIRCUITOS DIGITALES

De acuerdo a su complejidad, los circuitos integrados digitales se clasifican en 4 categorías básicas llamadas SSI, MSI, LSI, y VLSI. Esta clasificación se fundamenta en la cantidad de compuertas utilizadas para implementar la función propia del chip. Como sabemos, las compuertas son los bloques constructivos básicos de todos los circuitos Digitales.

SSI

Significa Small Scale Integration (integración en pequeña escala) y comprende los chips que contienen menos de 13 compuertas. Ejemplos: compuertas y flip-flops. Los CI SSI se fabrican principalmente empleando tecnologías TTL, CMOS y ECL. Los primeros circuitos integrados eran SSI

MSI

Significa Medium Scale Integration (integración en mediana escala) y comprende los chips que contiene de 13 a 100 compuertas. Ejemplos; codificadores, registros, contadores, multiplexores, decodificadores, demultiplexores. Los CI MSI se fabrican empleando tecnologías TTL, CMOS y ECL.

LSI

Significa Large Scale Integration (integración en alta escala) y comprende los chips que contienen de 100 a 1000 compuertas. Ejemplos: memorias, unidades aritméticas y lógicas (ALU's), microprocesadores de 8 y 16 bits. Los CI LSI se fabrican principalmente empleando tecnologías 12L, NMOS y PMOS.

VLSI

Significa Very Large Scale Integration (integración de muy alta escala) y comprende los chips que contienen más de 1000 compuertas, Ejemplos: microprocesadores de 32 bits, microcontroladores, sistemas de adquisición de datos. Los CI VLSI se fabrican también empleando tecnologías 12L, NMOS y PMOS.

FAMILIAS LOGICAS DE LOS CIRCUITOS INTEGRADOS

Una familia lógica es un conjunto de componentes digitales que comparten una tecnología común de Fabricación y tienen estandarizadas sus características de entrada y salida; es decir, son compatibles unos con otros.

Como consecuencia de la estandarización, la interconexión entre dispositivos lógicos de una misma familia es particularmente sencilla y directa: no requiere de etapas adicionales de acoplamiento.

CARACTERISTICAS GENERALES DE LAS FAMILIAS LÓGICAS

Todas las familias o tecnologías de fabricación de circuitos integrados digitales se agrupan en dos categorías generales: bipolares y MOS. Las características más relevantes de un circuito integrado digital con su velocidad, su consumo de potencia, su inmunidad al ruido y su confiabilidad. A continuación se definen estos términos, desde un punto de vista general.

La Velocidad

Mide la rapidez de respuesta de las salidas de un circuito digital a cualquier cambio en sus entradas. La velocidad es una consideración importante en el diseño de sistemas que deben realizar cálculos numéricos o en circuitos que trabajan con señales de alta frecuencia.

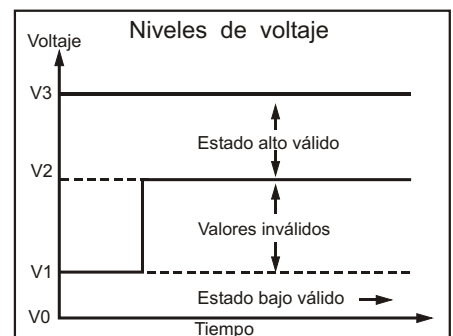
El consumo de potencia mide la cantidad de corriente o de potencia que consume un circuito digital en operación. El consumo de potencia es una consideración importante en el diseño de sistemas operados por baterías

La inmunidad al ruido

Mide la sensibilidad de un circuito digital al ruido electromagnético ambiental. La inmunidad al ruido es una consideración importante en el diseño de sistemas que deben trabajar en ambientes ruidosos como automóviles, máquinas, circuitos de control industrial, etc.

La confiabilidad

Mide el período útil de servicio de un circuito digital, es decir, cuánto tiempo se espera que trabaje sin fallar. Niveles de voltaje y estados lógicos. En todos los circuitos digitales prácticos los estados lógicos 1 y 0 se implementan con niveles de voltaje. Estos niveles tienen rangos muy definidos, separados por una zona de valores inválidos como se muestra en la figura siguiente



En esta figura, el nivel bajo válido es el rango de voltajes entre V_0 y V_1 , mientras que el nivel alto válido es el rango de voltajes entre V_2 y V_3 .

Los voltajes superiores a V_3 ó inferiores a V_0 son generalmente dañinos para los dispositivos digitales y deben evitarse. Generalmente, V_0 corresponde a un nivel de 0 voltios y V_3 al valor del voltaje de alimentación (5V, 9V, etc.).

La zona de niveles inválidos entre V1 y V2 es crítica. En esta área los circuitos digitales trabajan en forma errática porque no saben qué hacer. Un voltaje en ese rango puede ser interpretado como un 1 lógico o como un 0 lógico o no producir efectos alguno. Los niveles de voltaje en circuitos integrados digitales varían de acuerdo con la familia lógica (TTL o CMOS) a la que pertenece el dispositivo.

Como hemos visto anteriormente en la tabla anterior hay muchas familias lógicas en las cuales se diferencian por las características anteriores mencionadas pero que en este estudio veremos dos de las familias más utilizadas y más conocidas por su versatilidad y por su comodidad en el manejo de ellas mismas, las cuales son los TTL y los CMOS.

LA FAMILIA DE LOS TTL

La familia lógica TTL es quizás la más antigua y común de todas las familias lógicas de circuitos integrados digitales. La mayor parte de los chips SSI y MSI se fabrican utilizando tecnología TTL.

Los circuitos integrados TTL implementan su lógica interna, exclusivamente, a base de transistores NPN y PNP, diodos y resistencias.

La primera serie de dispositivos digitales TTL fue lanzada por Texas Instruments en 1964. Los chips TTL se usan en toda clase de aplicaciones digitales, desde el más sencillo computador personal hasta el más sofisticado robot industrial. Los circuitos TTL son rápidos, versátiles y muy económicos.

La familia TTL está disponible en dos versiones: la serie 54 y la serie 74. La primera se destina a las aplicaciones militares y la segunda a aplicaciones industriales y de propósito general. Los dispositivos de la serie 54 tienen rangos de operación de temperatura y voltaje más flexible (desde -55 hasta 125°C contra 0 a 70°C de la serie 74).

La familia TTL, o bipolar se divide en las siguientes Categorías o subfamilias básicas:

TTL STANDART

TTL SHOTTKY (S)

TTL DE BAJA POTENCIA (L)

TTL SHOTTKY DE BAJA POTENCIA (LS)

TTL DE ALTA VELOCIDAD (H)

TTL SHOTTKY AVANZAD (AS)

TTL SHOTTKY DE BAJA POTENCIA AVANZADA (ALS)

Otra familia bipolar muy popular es la ECL (Lógica de emisor acoplado). Los dispositivos de esta familia se caracterizan por su rapidez, pero consumen mucha potencia, son costosos y su manufactura es relativamente compleja. Su uso se limita a aplicaciones de muy alta velocidad.

TTL estandar

Estándar La familia estándar comprende principalmente los dispositivos que se designan como 74xx (7400, 7447, etc.). 74xxx (74123, 74193, etc.), 8xxx (8370, 8552, etc.) Y 96xx (9601, 9615, etc.), Trataremos con preferencia la 1ª serie 74xx y 74xxx que son las más utilizadas en los circuitos modernos.

Existe una gran cantidad de funciones lógicas que se realizan con esta tecnología. Entre las principales tenemos: compuertas, decodificadores, contadores, flip flop, sumadores, multiplexores y muchas otras que estudiaremos más adelante.

Características de los circuitos integrados TTL

Las características que más se notan de los circuitos integrados de la familia TTL, estándar son, los siguientes:

Alta velocidad de operación. Pueden trabajar con frecuencias de 18 a 20 Mhz y en algunas veces hasta 80 Mhz. La velocidad de operación se expresa casi siempre en términos del tiempo o retardo de propagación del CI.

El tiempo o retardo de propagación de un circuito digital es el tiempo que toma un cambio lógico en la entrada en propagarse a través del dispositivo y producir un cambio lógico en la salida.

Los tiempos de propagación en TTL normalmente del orden de 2 a 30 nanosegundos por compuerta.

Alta disipación de potencia. Es una desventaja asociada con la alta velocidad de operación. En general, cuanto más rápido sea un circuito, más potencia consume y viceversa. La mayoría de los circuitos TTL disipan típicamente, de 1 a 25 milivatios por compuerta.

Tensión de alimentación nominal de +5V. Los circuitos TTL en general pueden operar con tensiones de CC entre 4.75 y 5.25 V pero el valor nominal de la tensión de trabajo es +5 V. Por esta razón, los aparatos que incluyen circuitos integrados TTL se deben alimentar con una fuente regulada de 5 voltios.

Niveles de voltaje de 0 a 0.08 V para el estado bajo y de 2.4 a 5.0 V para el estado alto. En general, los circuitos TTL interpretan cualquier voltaje entre 0 y 0.8V como un cero (0) lógico o bajo y cualquier voltaje entre 2.4 y 5V como un (1) lógico o alto.

El máximo voltaje positivo que puede aplicarse a una entrada TTL es +5.5V y el máximo negativo es -0.5V. Al excederse estos parámetros, los dispositivos TTL generalmente se destruyen.

Abanicos de entrada (fan-in) y de salida (fan-out)

La familia TTL utiliza a dos parámetros para determinar cuántos dispositivos TTL se pueden conectar entre sí. Estos parámetros se denominan abanico de entrada (fan-in).

El fan-in mide el efecto de carga que presenta una entrada a una salida. Cada entrada de un circuito TTL estándar se comporta como una fuente de corriente capaz de suministrar 1.8 mA. A este valor de corriente se le asigna un fan-in de 1.

El fan-out mide la capacidad de una salida de manejar una o más entradas. Cada salida de un circuito TTL estándar se comporta como un disipador de corriente capaz de aceptar hasta 18 mA, es decir de manejar hasta 10 entradas TTL estándares. Por tanto, el fan-out de una salida TTL estándar es 10.

Existen dispositivos TTL especiales llamados buffers (separadores) y drivers (manejadores) que tienen fan-outs de 30, 50 r incluso 100. Se utilizan en aplicaciones donde una determinada línea de salida debe manejar al mismo tiempo un gran número de líneas de entrada. Los buffers y drivers se estudian en detalle en las lecciones 6 y 8.

Otros circuitos integrados TTL

Existen varias series o subfamilias TTL, además e la serie TTL estándar 74. Cada una de estas subfamilias posee características propias que las hacen adecuadas para aplicaciones o necesidades muy específicas. Las más conocidas son:

TTL de baja potencia. Comprenden los dispositivos designados como 74L00, 74L04. Consumen 10 veces menos potencia que los dispositivos TTL estándares correspondientes pero son 4 veces más lentos.

TTL de alta velocidad. Comprende los dispositivos designados como 74Hxx y 74Hxxx; por ejemplo: 74H05, 74H123. Consumen 2.5 veces más potencia que los dispositivos TTL estándares pero son 2 veces más rápidos.

TTL Shottky. Comprende los dispositivos designados como 74Sxx y 74Sxxx; por ejemplo 74S181, 74S11. Consumen 1.8 veces más potencia que los dispositivos TTL estándares pero son 4 veces más rápidos.

TTL Shottky de baja potencia. Comprende los dispositivos designados como 74LSxx 74LSxxx (74LS83, 74LS221, etc.). Consumen 5 veces menos potencia que los dispositivos TTL estándares y son igual de rápidos. Esta es la subfamilia más utilizada entre todas las divisiones de la familia TTL.

TTL Shottky avanzada de baja potencia. Comprende los dispositivos designados como 74ALSXX y 74ALSXXX; por ejemplo: 74ALS00, 74ALS73. Consumen la mitad de la potencia requerida por los dispositivos LS equivalentes y son el doble de rápidos.

TTL Shottky avanzada. Comprende los dispositivos designados como 74AS xx y 74ASxxx; por ejemplo 74AS00, 74AS73. Proporciona los más cortos tiempos de propagación que el estado actual de la tecnología bipolar puede ofrecer y su consumo es intermedio entre TTL estándar y LS.

ABREVIATURAS TÍPICAS DE LOS INTEGRADOS

H	= NIVEL LOGICO ALTO (ESTABLE)
L	= NIVEL LOGICO BAJO (ESTABLE)
↑	= FLANCO DE SUBIDA (paso de nivel lógico bajo a nivel alto)
↓	= FLANCO DE BAJADA (paso de nivel lógico alto a nivel alto)
X	= NIVEL DE ESTADO DIFERENTE
Z	= ESTADO DE ALTA IMPEDANCIA DE UNA SALIDA (LOGICA TRI-STATE)
a...h	= EL NIVEL LOGICO ESTABLE DE LAS ENTRADAS A...H
Qo	= SALIDAS DE FLIP FLOP
DATA INPUTS	= ENTRADA DE DATOS
ENABLE	= HABILITADOR
SELECT	= SELECTOR
CS	= SELECTOR DE ENCENDIDO O APAGADO
GND	= TIERRA
VCC	= VOLTAGE
DO....Dn	= ENTRADAS
CLOCK	= ENTRADA O SALIDA DEL RELOJ
INHIBIBIT-OUT	= INHABILITADOR DE SALIDA
SG	= SELECTOR DE GRUPO
OUTPUT	= SALIDA DE CONTROL

TTL Selector Guide

● AND Gates

Dual 4-Input
ECG74H21
ECG74LS21

Triple 3-Input
ECG7411
ECG74H11
ECG74HC11
ECG74LS11

Quad 2-Input
ECG7408
ECG74C08
ECG74HC08
ECG74HCT08
ECG74LS08
ECG74S08

● AND Gates with Open Collector Output

Triple 3-Input
ECG74LS15

Quad 2-Input
ECG7409
ECG74LS09

● AND/OR/Invert Gates

2-Wide 4-Input
ECG74LS55

Dual 2-Wide 2-Input
ECG74S51

Dual 2-Wide 2-2-3-2-Input
ECG74LS51

4-Wide 2-Input
ECG7454

4-Wide 2-2-3-2-Input
ECG74H54

4-Wide 3-2-2-3-Input
ECG74LS54

● Arithmetic & Logic Function Devices

Adders

1-Bit
ECG7480

4-Bit
ECG7483
ECG74LS83A
ECG74LS283

Look-Ahead Carry-Generator
ECG74182

True/Complement Zero/One Element
ECG74H87

4-Bit Arithmetic Logic Unit/Function Generator
ECG74181
ECG74LS181
ECG74S181

4-Bit Magnitude Comparator
ECG7485
ECG74C85
ECG74LS85

4 x 4 Register Files
ECG74170
ECG74LS670

6-Bit Binary Rate Multiplier
ECG7497

9-Bit Parity Generator/Checker
ECG74180
ECG74SL280

● Buffer Gates

Quad 2-Input NAND
ECG7437
ECG74LS37

Quad 2-Input NOR
ECG7428
ECG74LS28

Dual 4-Input NAND
ECG7440
ECG74H40
ECG74S40

● Buffer Gates with Open Collector Output

Hex
ECG7406
ECG7407
ECG7416
ECG7417

Quad
ECG74125
ECG74HC125
ECG74LS125A
ECG74126
ECG74HC126
ECG74LS126

Quad 2-Input NAND
ECG7438
ECG74LS38

Quad 2-Input NOR
ECG7433

● Buffers/Drivers

Hex Inverting
ECG7406
ECG7416
ECG80C96

Hex Non-Inverting
ECG7407
ECG7417
ECG80C95
ECG80C97

Octal Inverting
ECG74HC240
ECG74HCT240
ECG74LS240
ECG74LS540

Octal Non-Inverting
ECG74LS241
ECG74C244
ECG74HC244
ECG74HCT244
ECG74LS244
ECG74LS541

● Bus Drivers

Hex Inverting
ECG74366
ECG74LS366A
ECG74368
ECG74LS368
ECG80C96

Hex Non-Inverting

ECG74365
ECG74LS365A
ECG74367
ECG74LS367
ECG80C95
ECG80C97

● Bus Transceivers

Octal Inverting
ECG74LS640
ECG74LS642

Octal Inverting/Non-Inverting
ECG74LS643

Octal Non-Inverting
ECG74LS245
ECG74LS641
ECG74LS645

Quad Inverting
ECG74LS242

Quad Non-Inverting
ECG74LS243

● Counters, Asynchronous

Binary/Ripple
ECG74HC4060

Decade
ECG7490
ECG74C90
ECG74LS90
ECG74290
ECG74LS290

Dual Decade
ECG74HC390
ECG74LS390
ECG74490
ECG74LS490

4-Bit Binary
ECG7493A
ECG74C93
ECG74LS93
ECG74LS293

Dual 4-Bit Binary
ECG74393
ECG74HC393
ECG74LS393

Divide-By-N
ECG8520

Divide-By-12
ECG7492
ECG74LS92

● Counters, Synchronous

Decade
ECG74160
ECG74LS160A
ECG74162
ECG74LS162A

4-Bit Binary
ECG74161
ECG74C161
ECG74HC161
ECG74LS161A
ECG74HC163
ECG74HCT163
ECG74LS163A
ECG8316
ECG8556

TTL Selector Guide (cont'd)

● Counters, Up/Down

Decade

ECG74LS168A
ECG74LS190
ECG74C192
ECG74LS192

4-Bit Binary

ECG74LS169A
ECG74191
ECG74LS191
ECG74193
ECG74C193
ECG74LS193

● Counter/Latch

Decade

ECG74176
ECG74196
ECG74LS196

4-Bit Binary

ECG74177
ECG74LS197
ECG8554

● Data Selectors/Multiplexers

Dual 4-Line-to-1-Line

ECG74153
ECG74HC153
ECG74LS153
ECG74LS253
ECG74LS352
ECG74LS353
ECG8309

Quad 2-Line-to-1-Line

ECG74157
ECG74C157
ECG74LS157
ECG74158
ECG74LS158
ECG74HC257
ECG74LS257
ECG74LS258
ECG74S258
ECG8123
ECG8233

Quad 2-Line-to-1-Line with Storage

ECG74LS298

Quad 2-Line-to-1-Line (Open Collector)

ECG8235
ECG8266

8-Line-to-1-Line

ECG74C151
ECG74HC151
ECG74LS151
ECG74251
ECG74LS251
ECG74S251

16-Line-to-1-Line

ECG8219

● Decoder, 4-Line-to-10-Line

BCD-to-Decimal

ECG7442
ECG74C42
ECG74LS42

● Decoders/Demultiplexers

Dual 2-Line-to-4-Line

ECG74HC139
ECG74LS139
ECG74155
ECG74LS155
ECG8321

Dual 2-Line-to-4-Line (Open Collector)

ECG74156
ECG74LS156

4-Line-to-16-Line

ECG74154

3-Line-to-8-Line

ECG74HC138
ECG74HCT138
ECG74LS138
ECG74S138

● Display Decoders/Drivers

BCD-to-Decimal - Drives Cold Cathode Tubes

ECG74141

BCD-to-Decimal - Drives Gas Filled Tubes

ECG7441

BCD-to-Decimal (Open Collector)

ECG7445
ECG74145
ECG74LS145

BCD-to-7-Segment (Open Collector)

ECG7447
ECG74LS47
ECG74LS49
ECG74LS247
ECG74249
ECG74LS249

BCD-to-7-Segment

ECG7448
ECG74C48
ECG74LS48
ECG74LS248

● Display Decoder/Drivers with Input Latches

Hexadecimal-to-7-Segment - Drives Common Anode LED

ECG8374

● Encoders

Keyboard Encoders

ECG74C922
ECG74C923

8-Line-to-3-Line - Octal Priority Encoder

ECG74LS148
ECG74LS348
ECG8318

10-Line-to-4-Line - Decimal to BCD Priority Encoder

ECG74LS147

● Exclusive OR Gates

Quad 2-Input

ECG7486
ECG74H86
ECG74HC86
ECG74LS86
ECG74LS386

● Exclusive OR Gates with Open Collector Output

Quad 2-Input

ECG74136
ECG74LS136

● Exclusive NOR Gates with Open Collector Output

Quad 2-Input

ECG74LS266

● Expandable Gates

Dual 2-Wide Input AND/OR/Invert

ECG7450
ECG74H50

Dual 4-Input NOR

ECG7423

2-Wide 4-Input AND/OR/Invert

ECG74H55

4-Wide 2-2-3-2-Input AND/OR/Invert

ECG74H52
ECG74H53

● Expandable AND/OR/Invert Gates

Dual 2-Wide 2-Input

ECG7450
ECG74H50

2-Wide 4-Input

ECG74H55

4-Wide 2-2-3-2-Input

ECG74H52
ECG74H53

● Expander Gates

Triple 3-Input

ECG74H61

4-Wide 2-3-3-2-Input

ECG74H62

● Flip-Flops, Master-Slave (M-S) Types

Dual J-K

ECG7473
ECG74H73
ECG74H76
ECG74H78

Gated J-K

ECG74H71
ECG7472
ECG74H72

● Flip-Flops, J-K Edge Triggered Types

Dual J-K Negative Edge Triggered

ECG74C76
ECG74C107
ECG74LS73
ECG74LS78
ECG74H106
ECG74LS107
ECG74H108
ECG74LS112A
ECG74S112
ECG74LS113
ECG74S113
ECG74LS114

TTL Selector Guide (cont'd)

Dual J-K Positive Edge Triggered

ECG74109
ECG74HC109
ECG74LS109A

Gated J-K Positive Edge Triggered

ECG7470

Gated J-K Negative Edge Triggered

ECG74H102

● Flip-Flops, "D" Types

Dual

ECG7474
ECG74C74
ECG74H74
ECG74LS74A
ECG74S74

Hex

ECG74174
ECG74C174
ECG74HC174
ECG74HCT174
ECG74LS174
ECG74S174

Octal

ECG74HC273
ECG74HCT273
ECG74LS273
ECG74C374
ECG74HC374
ECG74HC574
ECG74HCT374
ECG74LS374
ECG74HC377

Quad

ECG74175
ECG74C175
ECG74HC175
ECG74LS175
ECG74LS379
ECG8613

● Interface Gates, Hi-Voltage with Open Collector Output

Hex Inverting

ECG7406
ECG7416

Hex Non-Inverting

ECG7407
ECG7417

Quad 2-Input NAND

ECG7426
ECG74LS26

● Interface Buffers, Level Shifting

Hex Non-Inverting

ECG74C902

● Inverters

Hex

ECG7404
ECG74C04
ECG74H04
ECG74HC04
ECG74HCT04
ECG74LS04
ECG74S04

● Inverters with Open Collector Output

Hex

ECG7405
ECG74LS05
ECG74S05
ECG7406
ECG7416

● Latches

Octal "D"

ECG74LS363
ECG74C373
ECG74HC373
ECG74HC573
ECG74HCT373
ECG74HCT573
ECG74LS373

Quad \bar{S} - \bar{R}

ECG74LS279

Quad Latch

ECG8314

4-Bit Bistable

ECG7475
ECG74LS75

8-Bit Addressable

ECG74HC259
ECG74LS259

● Level Shifters (See Interface Buffers)

● Line Drivers and Receivers

Dual 4-Input NAND 50 Ohm Line Driver

ECG74S140

Dual Differential Line Receiver

ECG9615

Octal Inverting Line Driver/Receiver

ECG74C240
ECG74HC240
ECG74HCT240
ECG74LS240
ECG74LS540

Octal Non-Inverting Line Driver/Receiver

ECG74LS241
ECG74C244
ECG74HC244
ECG74HCT244
ECG74LS244
ECG74LS541

Quad 2-Input NOR 50 Ohm Line Driver

ECG74128

● Multiplexers/Demultiplexers

ECG74HC4053
ECG74HC4067

● Multivibrators, Monostable (One Shots)

Monostable

ECG74121

Dual Retriggerable/Resettable Monostable

ECG8853
ECG9602

Retriggerable Monostable

ECG74122
ECG74LS122
ECG74221
ECG74C221
ECG74LS221
ECG9601

Dual Retriggerable Monostable

ECG74123
ECG74HC123
ECG74LS123

● NAND Gates

Quad 2-Input

ECG7400
ECG74C00
ECG74H00
ECG74HC00
ECG74HCT00
ECG74LS00
ECG74S00
ECG7437
ECG74LS37

Triple 3-Input

ECG7410
ECG74C10
ECG74H10
ECG74HC10
ECG74LS10

Dual 4-Input

ECG7420
ECG74C20
ECG74H20
ECG74LS20
ECG7440
ECG74H40
ECG74S40

Dual 5-Input

ECG8092

8-Input

ECG74C30
ECG74H30
ECG74LS30

13-Input

ECG74LS133
ECG74S133

● NAND Gates with Open Collector Output

Quad 2-Input

ECG74H01
ECG74LS01
ECG74LS03
ECG74S03
ECG7426
ECG74LS26
ECG7438
ECG74LS38

Triple 3-Input

ECG7412
ECG74LS12

Dual 4-Input

ECG7422
ECG74H22
ECG74LS22
ECG74S22

TTL Selector Guide (cont'd)

● NOR Gates

Quad 2-Input

ECG7402
ECG74C02
ECG74HC02
ECG74LS02
ECG74S02
ECG7428
ECG74LS28

Triple 3-Input

ECG7427
ECG74LS27

Dual 4-Input

ECG7425

Dual 5-Input

ECG74LS260

Expandable Dual 4-Input

ECG7423

● NOR Gates with Open Collector Output

Quad 2-Input

ECG7433

● OR Gates

Quad 2-Input

ECG7432
ECG74C32
ECG74HC32
ECG74HCT32
ECG74LS32

● Registers

Quad I/O

ECG8542

4-Bit "D"

ECG74C173
ECG74HC173
ECG74LS173

4-Bit x 16 Word FIFO

ECG74HC40105

● Schmitt Triggers

Dual 4-Input NAND

ECG7413
ECG74LS13

Hex Inverter

ECG7414
ECG74C14
ECG74HC14
ECG74HCT14
ECG74LS14

Quad 2-Input NAND

ECG74132
ECG74HC132
ECG74LS132

● Shift Registers

4-Bit Parallel

ECG74195
ECG74LS195A

4-Bit Universal

ECG74LS395A

4-Bit Bidirectional Universal

ECG74LS194A
ECG74S194
ECG74LS295A

4-Bit Bidirectional Parallel

ECG7495
ECG74C95
ECG74LS95B

5-Bit Serial-In/Parallel-Out or Parallel-In/Serial-Out

ECG7496

8-Bit Serial

ECG7491
ECG74LS91

8-Bit Serial-in/Parallel-Out

ECG74164
ECG74C164
ECG74HC164
ECG74LS164

8-Bit Parallel-In/Serial-Out

ECG74165
ECG74HC165

8-Bit Universal

ECG74199

8-Bit Bidirectional Universal

ECG74198
ECG74HC299
ECG74LS299

8-Bit Serial or Parallel-In/Parallel-Out

ECG74166
ECG74LS166

Dual 8-Bit Serial

ECG8328

● Voltage Controlled Oscillators (VCO)

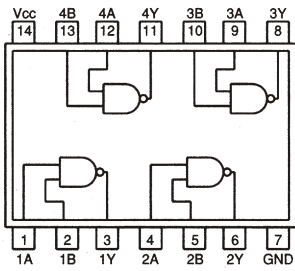
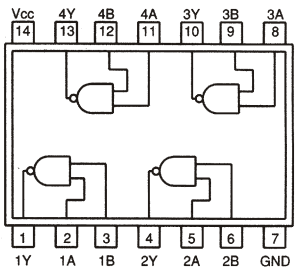
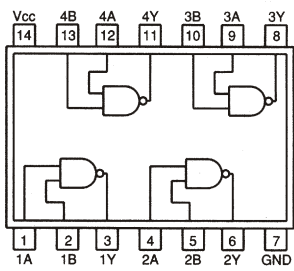
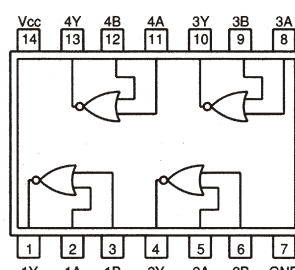
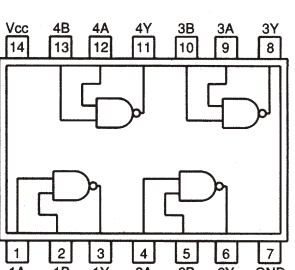
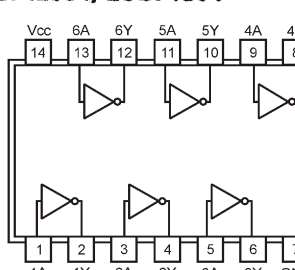
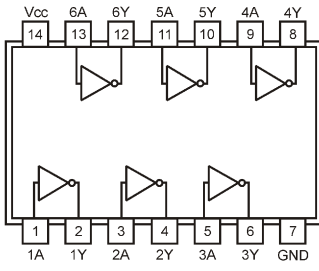
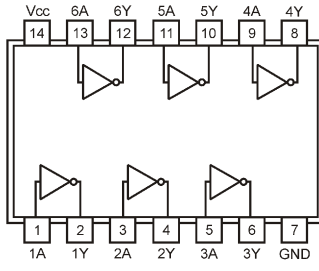
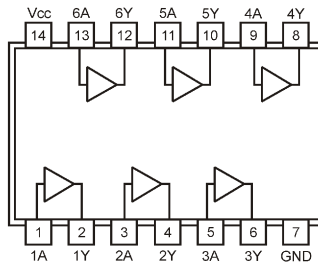
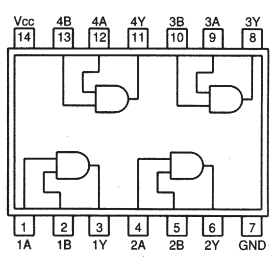
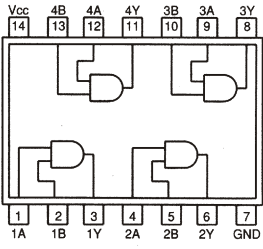
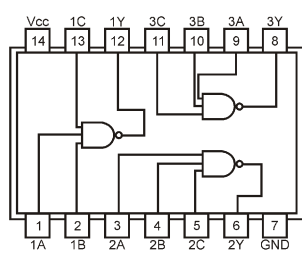
Single

ECG74LS624

Dual

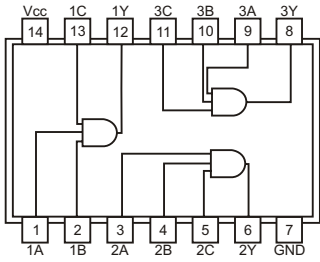
ECG74S124
ECG74LS625
ECG74LS626
ECG74LS627
ECG74LS629

TTL Logic Diagrams ($V_{CC} = +5\text{ V Nom.}$)

<p>Diag. 1 14-Pin DIP See Fig. D6 ECG7400, ECG74C00, ECG74H00, ECG74HC00, ECG74HCT00, ECG74LS00, ECG74S00</p>  <p>Quad 2-Input NAND Gate</p>	<p>Diag. 2 14-Pin DIP See Fig. D6 (See Also Diag. 3) ECG7401*, ECG74LS01</p>  <p>Quad 2-Input NAND Gate with Open Collector Output</p> <p>* DISCONTINUED</p>	<p>Diag. 3 14-Pin DIP See Fig. D6 (See Also Diag. 2) ECG74H01</p>  <p>Quad 2-Input NAND Gate with Open Collector Output</p>
<p>Diag. 4 14-Pin DIP See Fig. D6 ECG7402, ECG74C02, ECG74HC02, ECG74LS02, ECG74S02</p>  <p>Quad 2-Input NOR Gate</p>	<p>Diag. 5 14-Pin DIP See Fig. D6 ECG74LS03, ECG74S03</p>  <p>Quad 2-Input NAND Gate with Open Collector Output</p>	<p>Diag. 6 14-Pin DIP See Fig. D6 ECG7404, ECG74C04, ECG74H04, ECG74HC04, ECG74HCT04, ECG74LS04, ECG74S04</p>  <p>Hex Inverter</p>
<p>Diag. 7 14-Pin DIP See Fig. D6 ECG7405, ECG74H05, ECG74LS05, ECG74S05</p>  <p>Hex Inverter with Open Collector Output</p>	<p>Diag. 8 14-Pin DIP See Fig. D6 ECG7406</p>  <p>Hex Inverter/Buffer with Hi-Volt (30 V) Open Collector Output</p>	<p>Diag. 9 14-Pin DIP See Fig. D6 ECG7407</p>  <p>Hex Buffer with Hi-Volt (30 V) Open Collector Output</p>
<p>Diag. 10 14-Pin DIP See Fig. D6 ECG7408, ECG74C08, ECG74H08*, ECG74HC08, ECG74HCT08, ECG74LS08, ECG74S08</p>  <p>Quad 2-Input AND Gate</p> <p>* DISCONTINUED</p>	<p>Diag. 11 14-Pin DIP See Fig. D6 ECG7409, ECG74LS09, ECG74S09*</p>  <p>Quad 2-Input AND Gate with Open Collector Output</p> <p>* DISCONTINUED</p>	<p>Diag. 12 14-Pin DIP See Fig. D6 ECG7410, ECG74C10, ECG74H10, ECG74HC10, ECG74LS10, ECG74S10</p>  <p>Triple 3-Input NAND Gate</p>

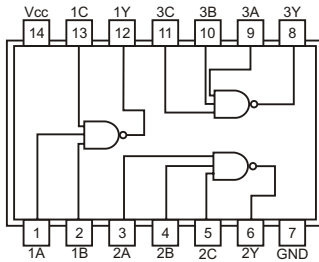
TTL Logic Diagrams (cont'd)

Diag. 13 14-Pin DIP See Fig. D6
**ECG7411, ECG74H11, ECG74HC11,
 ECG74LS11, ECG74S11**



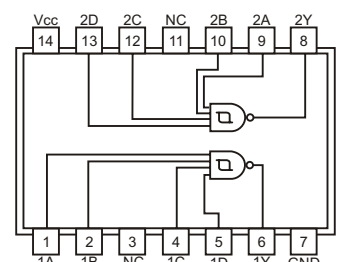
Triple 3-Input AND Gate

Diag. 14 14-Pin DIP See Fig. D6
ECG7412, ECG74LS12



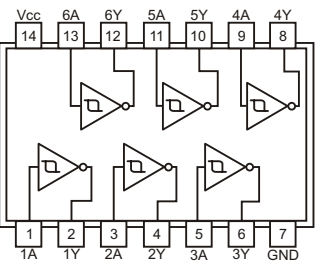
Triple 3-Input NAND Gate with Open Collector Output

Diag. 15 14-Pin DIP See Fig. D6
ECG7413, ECG74LS13



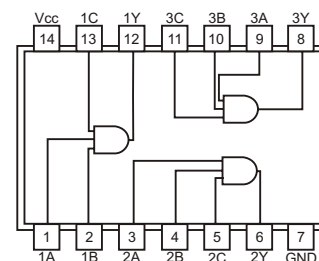
Dual 4-Input NAND Schmitt Trigger

Diag. 16 14-Pin DIP See Fig. D6
**ECG7414, ECG74C14, ECG74HC14,
 ECG74HCT14, ECG74LS14**



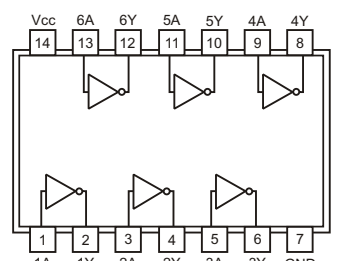
Hex Schmitt Trigger Inverter

Diag. 17 14-Pin DIP See Fig. D6
ECG74LS15



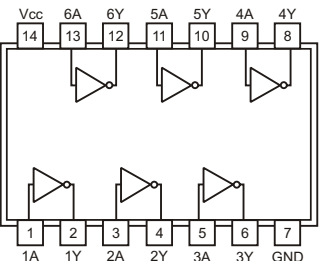
Triple 3-Input AND Gate with Open Collector Output

Diag. 18 14-Pin DIP See Fig. D6
ECG7416



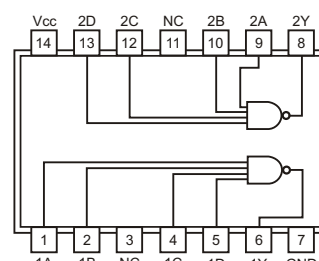
Hex Inverter/Buffer with Hi-Volt (15 V) Open Collector Output

Diag. 19 14-Pin DIP See Fig. D6
ECG7417



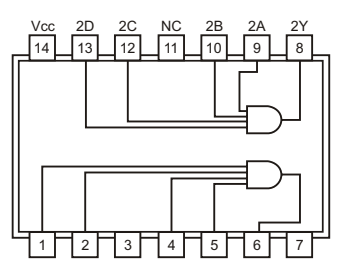
Hex Buffer with Hi-Volt (15 V) Open Collector Output

Diag. 20 14-Pin DIP See Fig. D6
**ECG7420, ECG74C20, ECG74H20*,
 ECG74LS20**



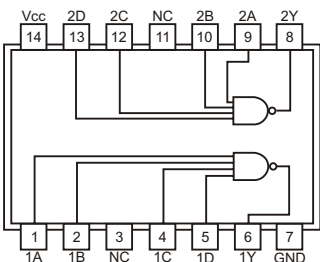
Dual 4-Input NAND Gate
 * DISCONTINUED

Diag. 21 14-Pin DIP See Fig. D6
ECG7421*, ECG74H21, ECG74LS21



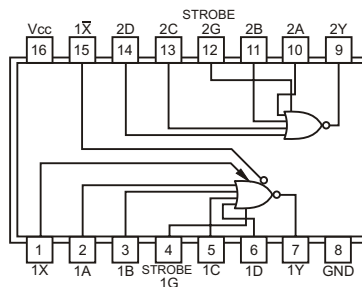
Dual 4-Input AND Gate
 * DISCONTINUED

Diag. 22 14-Pin DIP See Fig. D6
**ECG7422, ECG74H22*, ECG74LS22,
 ECG74S22**



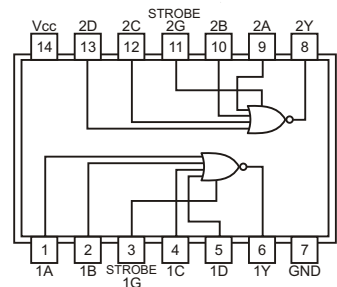
Dual 4-Input NAND Gate with Open Collector Output
 * DISCONTINUED

Diag. 23 16-Pin DIP See Fig. D8
ECG7423



Expandable Dual 4-Input NOR Gate with Strobe

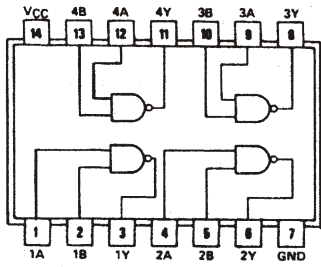
Diag. 24 14-Pin DIP See Fig. D6
ECG7425



Dual 4-Input NOR Gate with Strobe

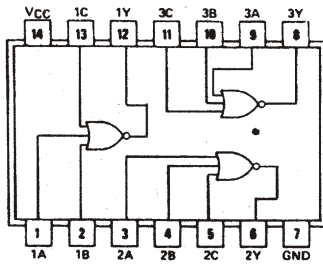
TTL Logic Diagrams (cont'd)

Diag. 25 14-Pin DIP See Fig. D6
ECG7426, ECG74LS26



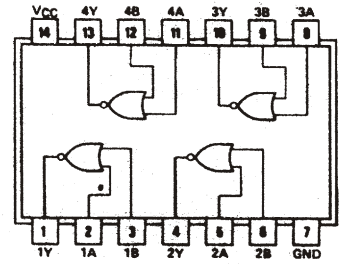
Quad 2-Input Hi-Volt Interface NAND Gate with Open Collector Output

Diag. 26 14-Pin DIP See Fig. D6
ECG7427, ECG74LS27



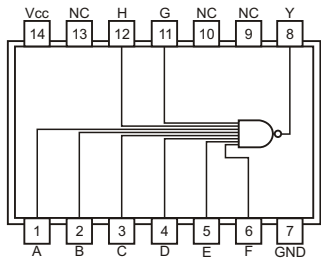
Triple 3-Input NOR Gate

Diag. 27 14-Pin DIP See Fig. D6
ECG7428, ECG74LS28



Quad 2-Input NOR Buffer

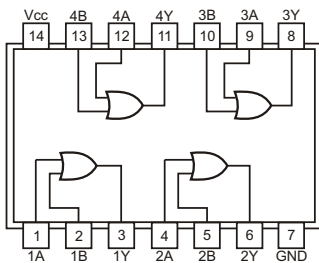
Diag. 28 14-Pin DIP See Fig. D6
ECG74C30, ECG74HC30*, ECG74LS30



8-Input NAND Gate

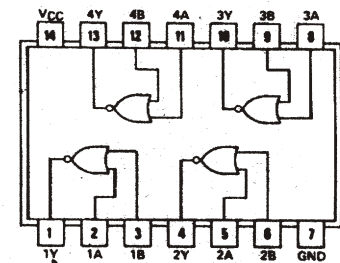
* DISCONTINUED

Diag. 29 14-Pin DIP See Fig. D6
ECG7432, ECG74C32, ECG74HC32, ECG74HCT32, ECG74LS32



Quad 2-Input OR Gate

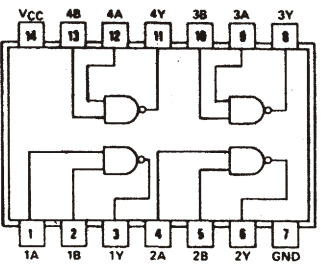
Diag. 30 14-Pin DIP See Fig. D6
ECG7433, ECG74LS33*



Quad 2-Input NOR Buffer with Open Collector Output

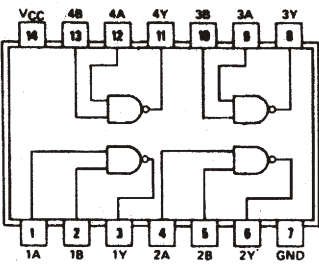
* DISCONTINUED

Diag. 31 14-Pin DIP See Fig. D6
ECG7437, ECG74LS37



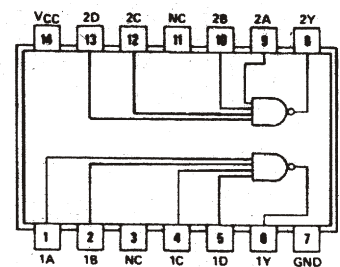
Quad 2-Input NAND Buffer

Diag. 32 14-Pin DIP See Fig. D6
ECG7438, ECG74LS38



Quad 2-Input NAND Buffer with Open Collector Output

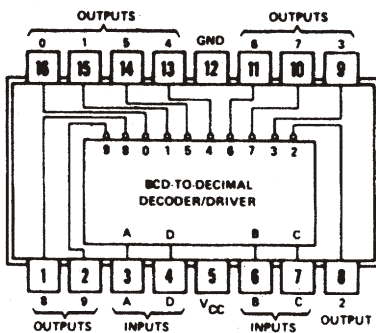
Diag. 34 14-Pin DIP See Fig. D6
ECG7440, ECG74H40, ECG74LS40*, ECG74S40



Dual 4-Input NAND Buffer

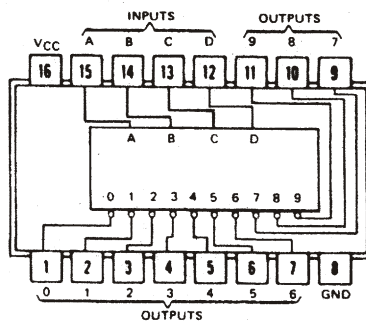
* DISCONTINUED

Diag. 35 16-Pin DIP See Fig. D8
ECG7441



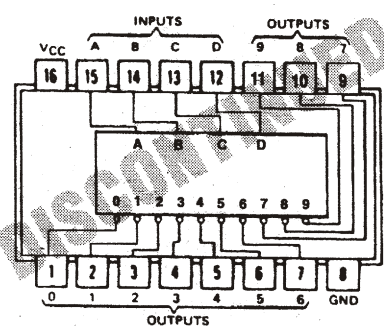
BCD-to-Decimal Decoder/Driver for Gas Filled Tubes

Diag. 36 16-Pin DIP See Fig. D8
ECG7442, ECG74C42, ECG74LS42



BCD-to-Decimal Decoder

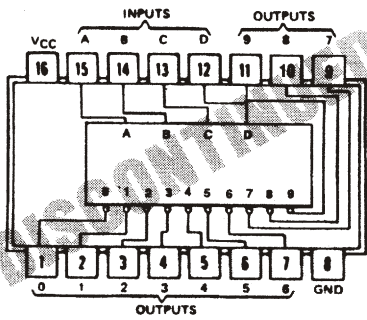
Diag. 37 16-Pin DIP See Fig. D8
ECG7443



Excess-3-to-Decimal Decoder

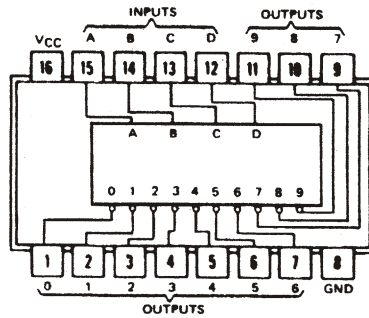
TTL Logic Diagrams (cont'd)

Diag. 38 16-Pin DIP See Fig. D8
ECG7444



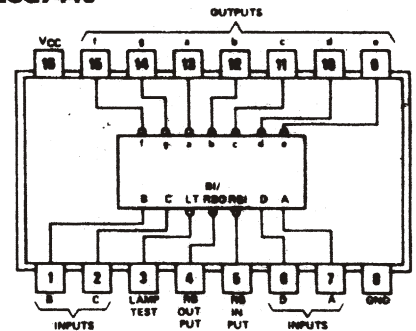
Excess-3-Gray-to-Decimal Decoder

Diag. 39 16-Pin DIP See Fig. D8
ECG7445



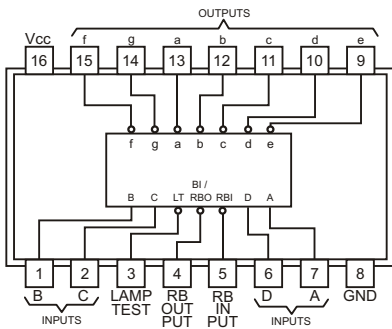
BCD-to-Decimal Decoder/Driver with Open Collector Output

Diag. 40 16-Pin DIP See Fig. D8
ECG7446



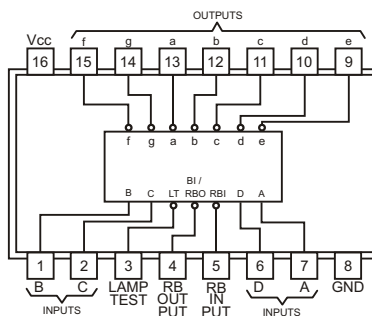
BCD-to-7-Segment Decoder/Driver with Hi-Volt (30 V) Open Collector Output

Diag. 41 16-Pin DIP See Fig. D8
ECG7447, ECG74LS47



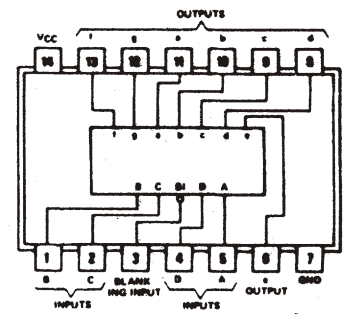
BCD-to-7-Segment Decoder/Driver with Hi-Volt (15 V) Open Collector Output

Diag. 42 16-Pin DIP See Fig. D8
ECG7448, ECG74C48, ECG74LS48



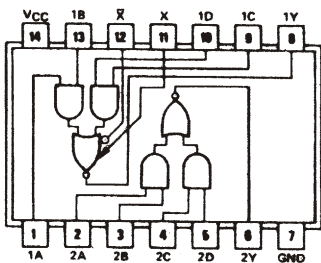
BCD-to-7-Segment Decoder/Driver

Diag. 43 14-Pin DIP See Fig. D6
ECG74LS49



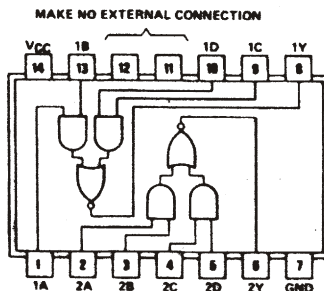
BCD-to-7-Segment Decoder/Driver with Open Collector Output

Diag. 44 14-Pin DIP See Fig. D6
ECG7450, ECG74H50



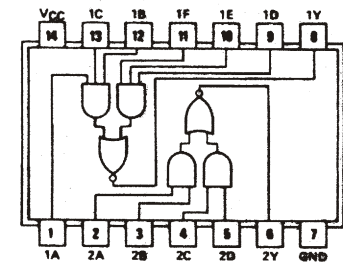
Dual 2-Wide 2-Input AND/OR/Invert Gate (One Gate Expandable)

Diag. 45 14-Pin DIP See Fig. D6 (See also Diag. 46)
ECG7451*, ECG74S51



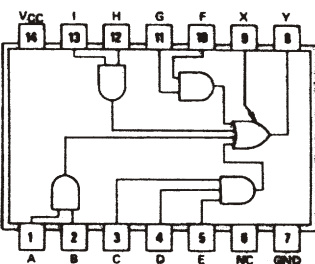
Dual 2-Wide 2-Input AND/OR/Invert Gate * DISCONTINUED

Diag. 46 14-Pin DIP See Fig. D6 (See also Diag. 45)
ECG74LS51



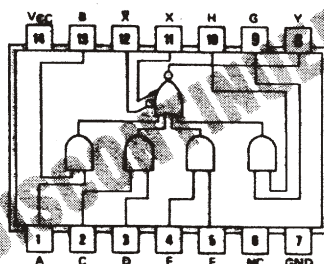
Dual 2-Wide 2-Input, 2-Wide 3-Input AND/OR/Invert Gate

Diag. 47 14-Pin DIP See Fig. D6
ECG74H52



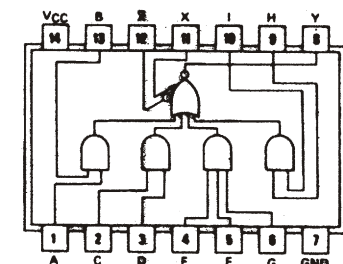
Expandable 4-Wide 2-Input 2-3-2-2 Input AND/OR Gate

Diag. 48 14-Pin DIP See Fig. D6 (See also Diag. 49)
ECG7453



Expandable 4-Wide 2-Input AND/OR/Invert Gate

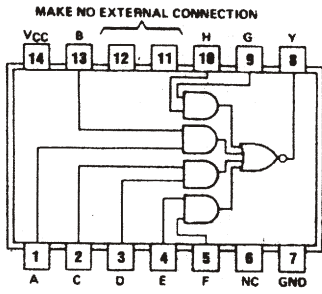
Diag. 49 14-Pin DIP See Fig. D6 (See also Diag. 48)
ECG74H53



Expandable 4-Wide 2-Input 2-2-3-2 Input AND/OR/Invert Gate

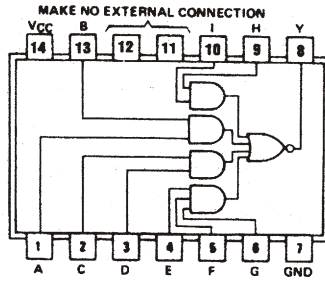
TTL Logic Diagrams (cont'd)

Diag. 50 14-Pin DIP See Fig. D6
(See also Diag. 51 and 52)
ECG7454



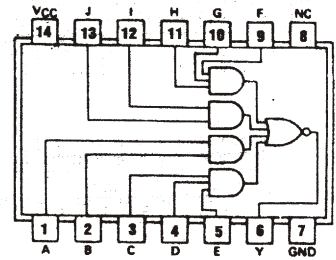
4-Wide 2-Input AND/OR/Invert Gate

Diag. 51 14-Pin DIP See Fig. D6
(See also Diag. 50 and 52)
ECG74H54



4-Wide 2-2-2-3 Input AND/OR/Invert Gate

Diag. 52 14-Pin DIP See Fig. D6
(See also Diag. 50 and 51)
ECG74LS54



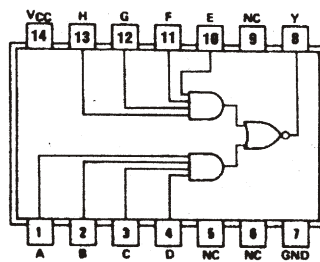
4-Wide 3-2-2-3 Input AND/OR/Invert Gate

Diag. 53 14-Pin DIP See Fig. D6
(See also Diag. 54)
ECG74H55



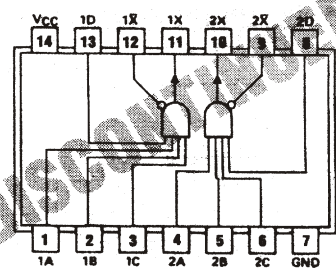
Expandable 2-Wide 4-Input AND/OR/Invert Gate

Diag. 54 14-Pin DIP See Fig. D6
(See also Diag. 53)
ECG74LS55



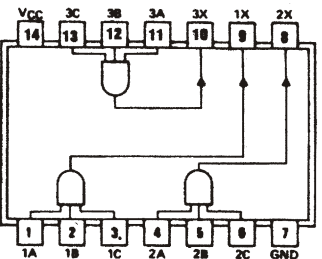
2-Wide 4-Input AND/OR/Invert Gate

Diag. 55 14-Pin DIP See Fig. D6
ECG7460



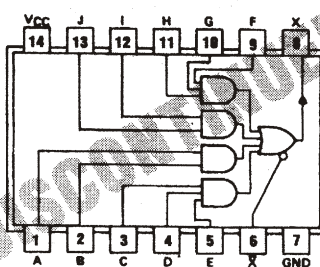
Dual 4-Input Expander

Diag. 56 14-Pin, DIP See Fig. D6
ECG74H61



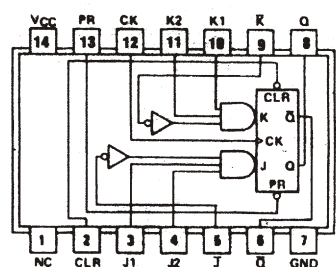
Triple 3-Input Expander

Diag. 57 14-Pin DIP See Fig. D6
ECG74H62



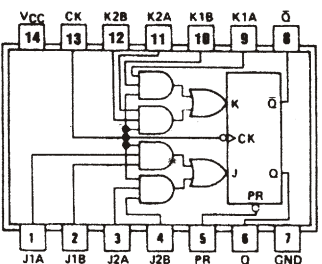
4-Wide 3-2-2-3 Input AND/OR Expander

Diag. 60 14-Pin DIP See Fig. D6
ECG7470



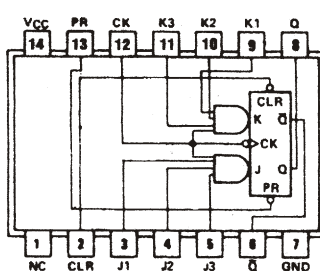
Gated J-K Positive Edge Triggered Flip-Flop with Preset and Clear

Diag. 61 14-Pin DIP See Fig. D6
ECG74H71



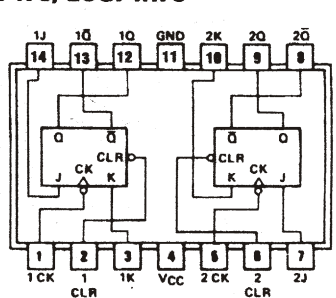
Gated J-K M/S Flip-Flop with Preset

Diag. 62 14-Pin DIP See Fig. D6
ECG7472, ECG74H72



Gated J-K M/S Flip-Flop with Preset and Clear

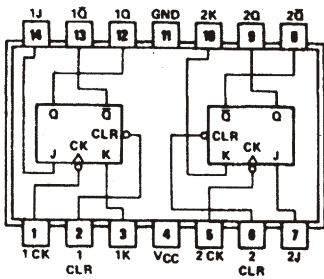
Diag. 63 14-Pin DIP See Fig. D6
(See also Diag. 64)
ECG7473, ECG74H73



Dual J-K M/S Flip-Flop with Clear

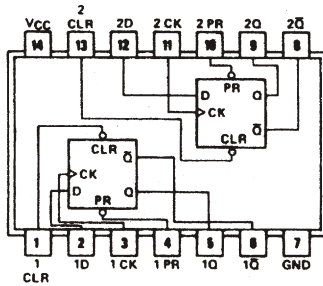
TTL Logic Diagrams (cont'd)

Diag. 64 14-Pin DIP See Fig. D6
(See also Diag. 63)
ECG74C73, ECG74LS73



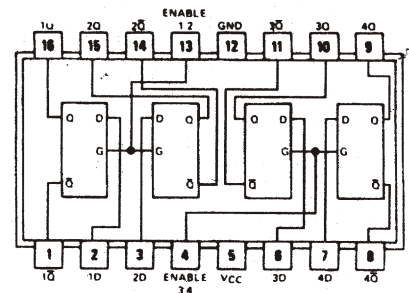
Dual J-K Negative Edge Triggered Flip-Flop with Clear

Diag. 65 14-Pin DIP See Fig. D6
ECG7474, ECG74C74, ECG74H74, ECG74LS74A, ECG74S74



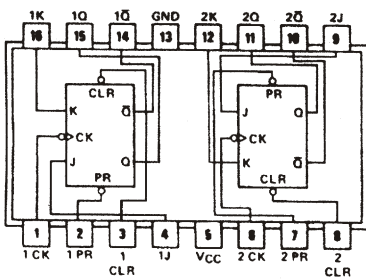
Dual "D" Flip-Flop with Preset and Clear

Diag. 66 16-Pin DIP See Fig. D8
ECG7475, ECG74LS75



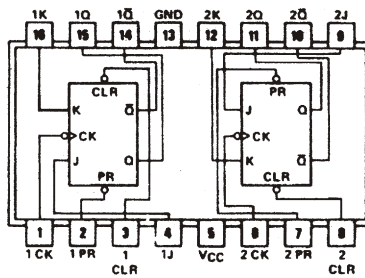
4-Bit Bistable Latch with Complementary Output

Diag. 67 16-Pin DIP See Fig. D8
(See also Diag. 68)
ECG74H76



Dual J-K M/S Flip-Flop with Preset and Clear

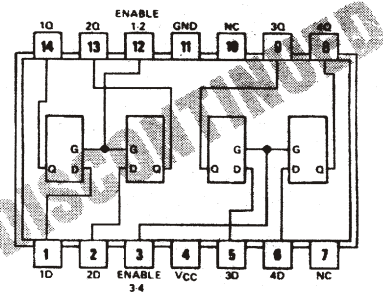
Diag. 68 16-Pin DIP See Fig. D8
(See also Diag. 67)
ECG74C76, ECG74LS76A*



Dual J-K Negative Edge Triggered Flip-Flop with Preset and Clear

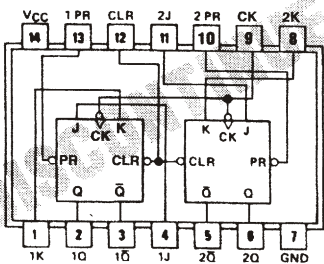
* DISCONTINUED

Diag. 69 14-Pin DIP See Fig. D6
ECG74LS77



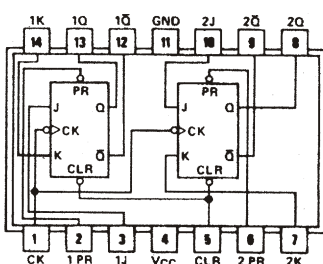
4-Bit Bistable Latch

Diag. 70 14-Pin DIP See Fig. D6
(See also Diag. 71)
ECG74H78



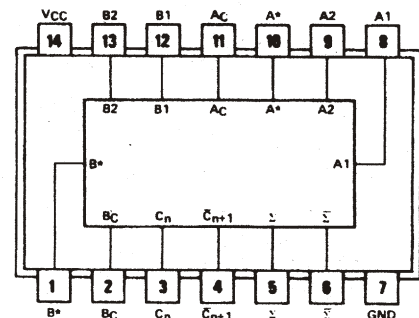
Dual J-K M/S Flip-Flop with Presets and a Common Clock and Clear

Diag. 71 14-Pin DIP See Fig. D6
(See also Diag. 70)
ECG74LS78



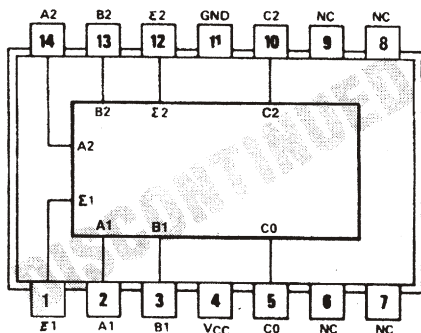
Dual J-K Negative Edge Triggered Flip-Flop with Preset and a Common Clock and Clear

Diag. 72 14-Pin DIP See Fig. D6
ECG7480



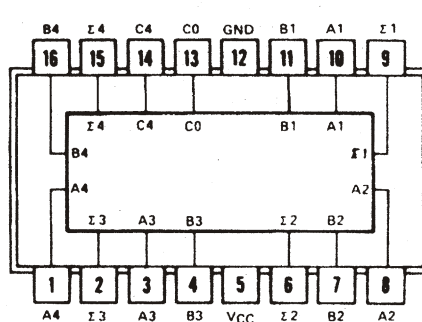
Gated Full Adder with Complementary Sum Outputs

Diag. 74 14-Pin DIP See Fig. D6
ECG7482



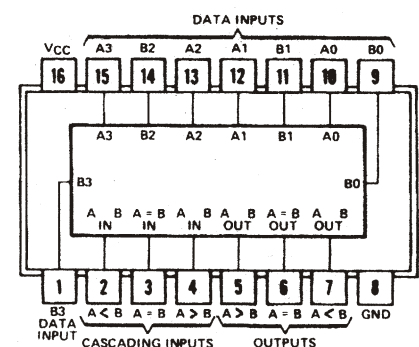
2-Bit Binary Full Adder

Diag. 75 16-Pin DIP See Fig. D8
ECG7483, ECG74LS83A



4-Bit Full Adder

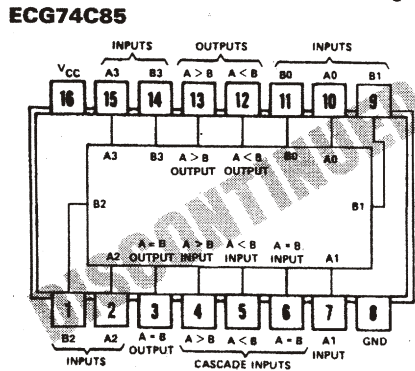
Diag. 76 16-Pin DIP See Fig. D8
ECG7485, ECG74LS85



4-Bit Magnitude Comparator

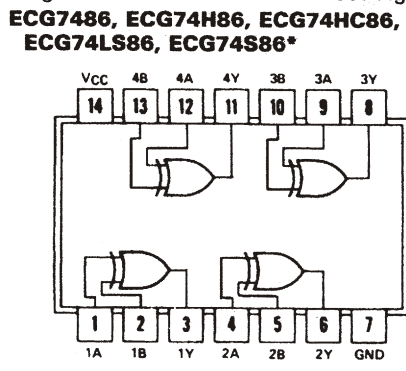
TTL Logic Diagrams (cont'd)

Diag. 77 16-Pin DIP See Fig. D8



4-Bit Magnitude Comparator

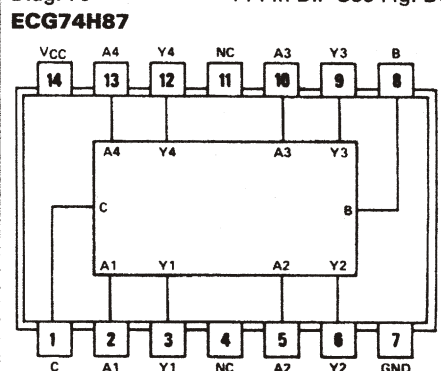
Diag. 78 14-Pin DIP See Fig. D6



Quad Exclusive OR Gate

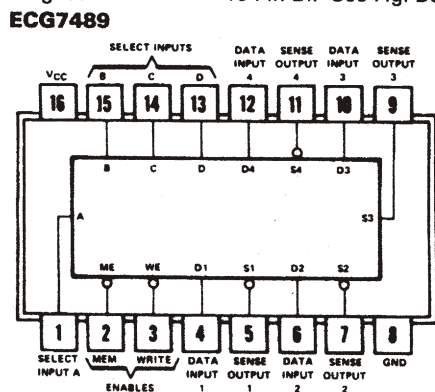
* DISCONTINUED

Diag. 79 14-Pin DIP See Fig. D6



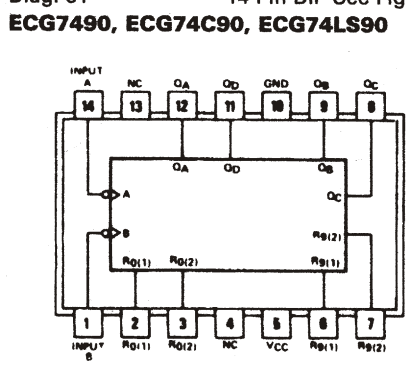
4-Bit True/Complement Zero/One Element

Diag. 80 16-Pin DIP See Fig. D8



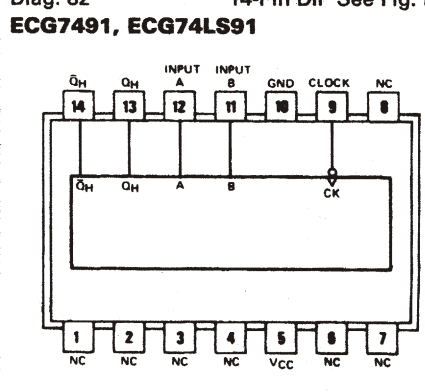
64-Bit RAM (16 x 4)

Diag. 81 14-Pin DIP See Fig. D6



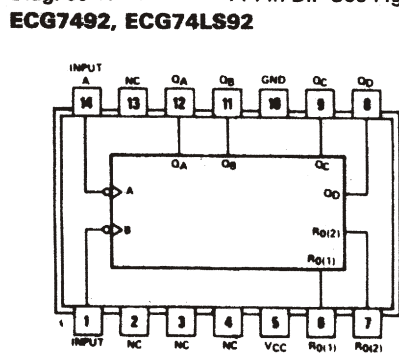
Decade Counter

Diag. 82 14-Pin DIP See Fig. D6



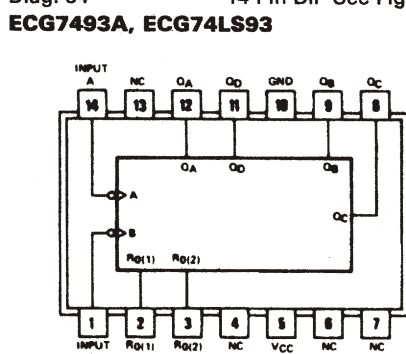
8-Bit Serial Shift Register

Diag. 83 14-Pin DIP See Fig. D6



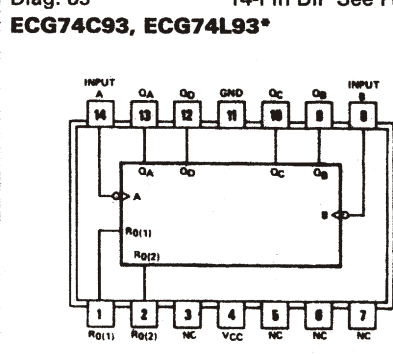
Divide-by-12 Counter

Diag. 84 14-Pin DIP See Fig. D6



4-Bit Binary Counter

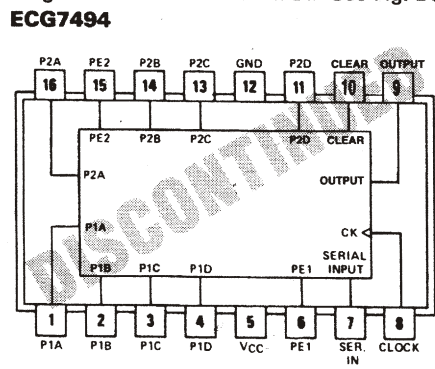
Diag. 85 14-Pin DIP See Fig. D6



4-Bit Binary Counter

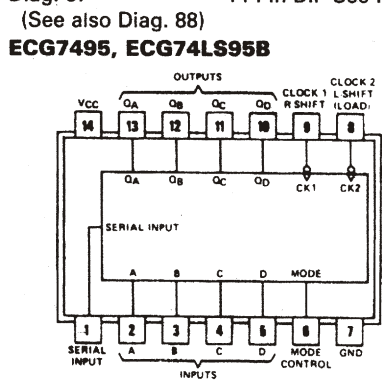
* DISCONTINUED

Diag. 86 16-Pin DIP See Fig. D8



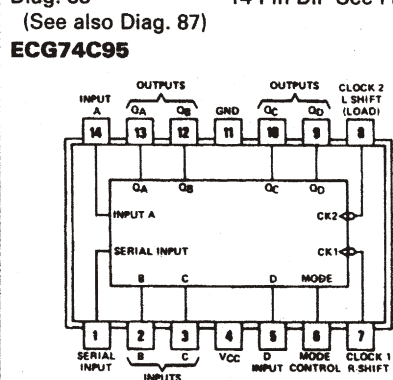
4-Bit Serial or Parallel Shift Register

Diag. 87 14-Pin DIP See Fig. D6



4-Bit Bidirectional or Parallel Shift Register

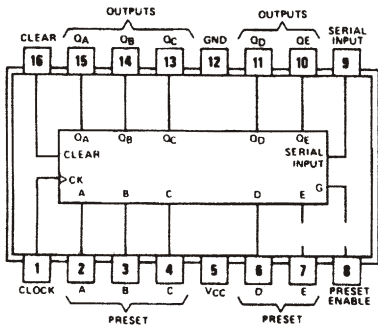
Diag. 88 14-Pin DIP See Fig. D6



4-Bit Bidirectional Parallel Shift Register

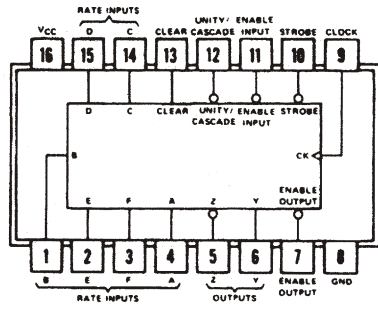
TTL Logic Diagrams (cont'd)

Diag. 89 16-Pin DIP See Fig. D8
ECG7496



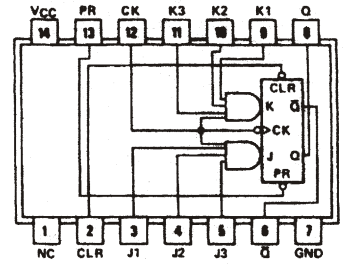
5-Bit Serial-In/Parallel-Out or Parallel-In/Serial-Out Shift Register

Diag. 90 16-Pin DIP See Fig. D8
ECG7497



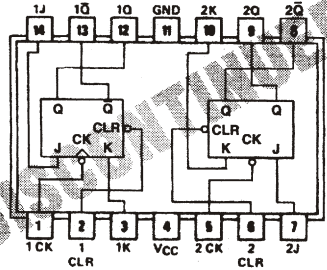
Synchronous 6-Bit Binary Rate Multiplier

Diag. 92 14-Pin DIP See Fig. D6
ECG74H102



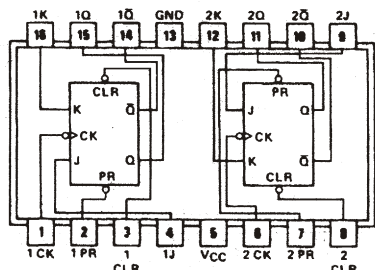
Gated J-K Negative Edge Triggered Flip-Flop with Preset and Clear

Diag. 93 14-Pin DIP See Fig. D6
ECG74H103



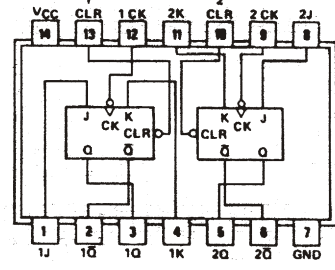
Dual J-K Negative Edge Triggered Flip-Flop with Clear

Diag. 94 16-Pin DIP See Fig. D8
ECG74H106



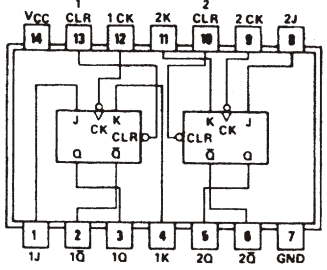
Dual J-K Negative Edge Triggered Flip-Flop with Clear

Diag. 95 14-Pin DIP See Fig. D6
(See also Diag. 96)
ECG74107



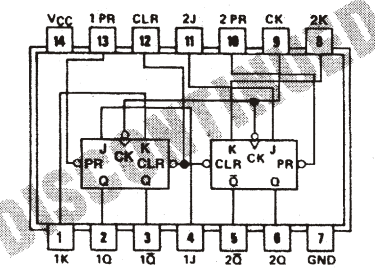
Dual J-K M/S Flip-Flop with Clear

Diag. 96 14-Pin DIP See Fig. D6
(See also Diag. 95)
ECG74C107, ECG74LS107



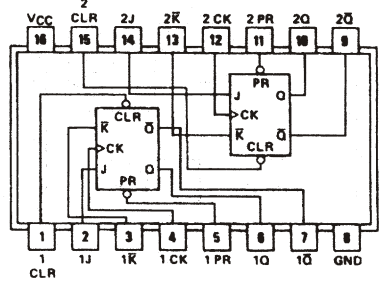
Dual J-K Negative Edge Triggered Flip-Flop with Clear

Diag. 97 14-Pin DIP See Fig. D6
ECG74H108



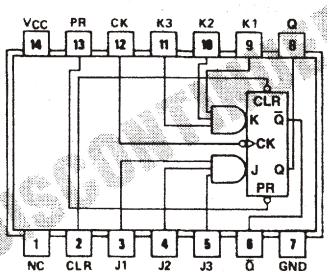
Dual J-K Negative Edge Triggered Flip-Flop with Clear

Diag. 98 16-Pin DIP See Fig. D8
ECG74109, ECG74HC109, ECG74LS109A



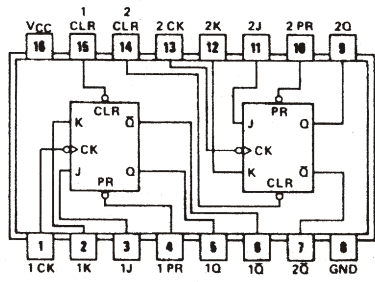
Dual J-K Positive Edge Triggered Flip-Flop with Preset and Clear

Diag. 99 14-Pin DIP See Fig. D6
ECG74110



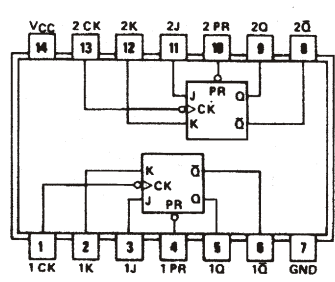
Gated J-K M/S Flip-Flop with Preset and Clear

Diag. 101 16-Pin DIP See Fig. D8
ECG74LS112A, ECG74S112



Dual J-K Negative Edge Triggered Flip-Flop with Preset and Clear

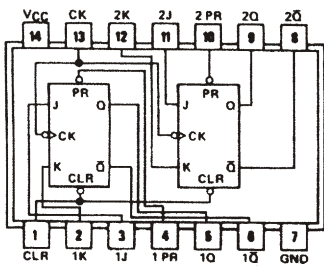
Diag. 102 14-Pin DIP See Fig. D6
ECG74LS113, ECG74S113



Dual J-K Negative Edge Triggered Flip-Flop with Preset

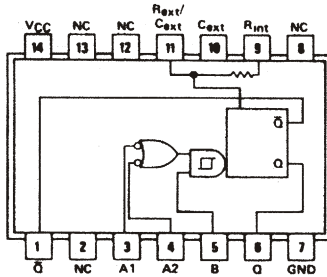
TTL Logic Diagrams (cont'd)

Diag. 103 14-Pin DIP See Fig. D6
ECG74LS114, ECG74S114



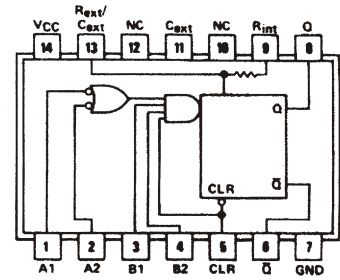
Dual J-K Negative Edge Triggered Flip-Flop with Presets and a Common Clock and Clear

Diag. 104 14-Pin DIP See Fig. D6
ECG74121



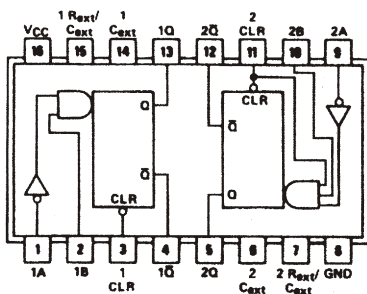
Monostable Multivibrator

Diag. 105 14-Pin DIP See Fig. D6
ECG74122, ECG74LS122



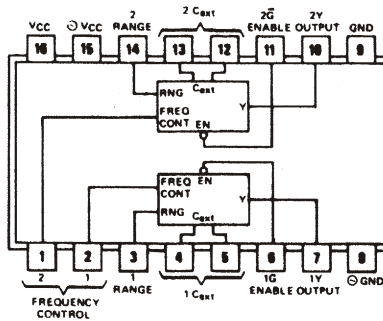
Retriggerable Monostable Multivibrator with Clear

Diag. 106 16-Pin DIP See Fig. D8
ECG74123, ECG74HC123, ECG74LS123



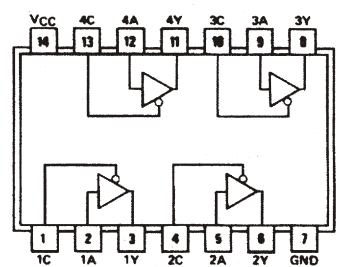
Dual Retriggerable Monostable Multivibrator with Clear

Diag. 107 16-Pin DIP See Fig. D8
ECG74S124



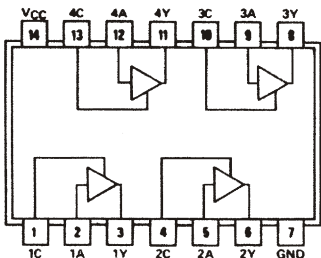
Dual Voltage Controlled Oscillator

Diag. 108 14-Pin DIP See Fig. D6
ECG74125, ECG74HC125, ECG74LS125A



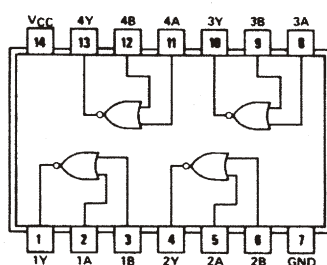
Quad Bus Buffer with 3-State Output (Active Low)

Diag. 109 14-Pin DIP See Fig. D6
ECG74126, ECG74HC126, ECG74LS126



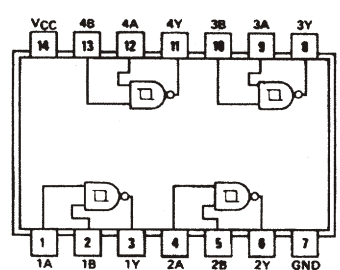
Quad Bus Buffer with 3-State Output (Active High)

Diag. 110 14-Pin DIP See Fig. D6
ECG74128



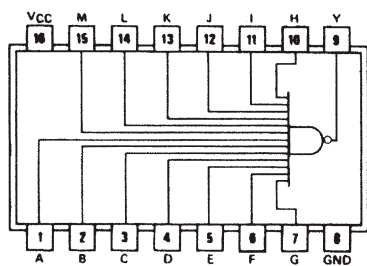
Quad 2-Input NOR 50 Ohm Line Driver

Diag. 111 14-Pin DIP See Fig. D6
ECG74132, ECG74HC132, ECG74LS132



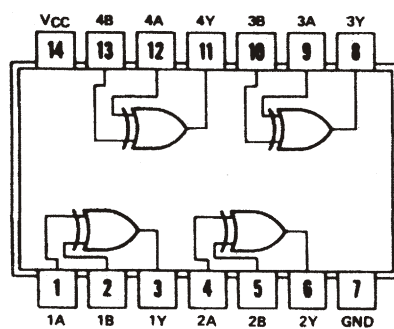
Quad 2-Input NAND Schmitt Trigger

Diag. 112 16-Pin DIP See Fig. D8
ECG74LS133, ECG74S133



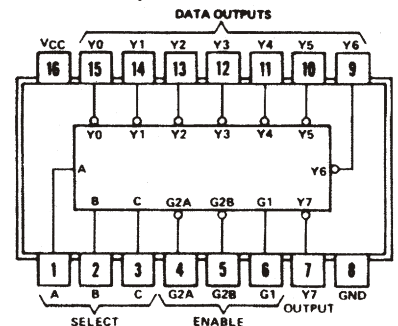
13-Input NAND Gate

Diag. 114 14-Pin DIP See Fig. D6
ECG74136, ECG74LS136



Quad Exclusive OR Gate with Open Collector Output

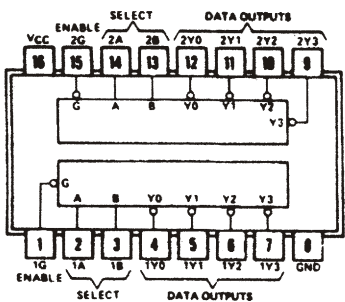
Diag. 115 16-Pin DIP See Fig. D8
ECG74HC138, ECG74HCT138, ECG74LS138, ECG74S138



3-Line-to-8-Line Decoder/Demultiplexer

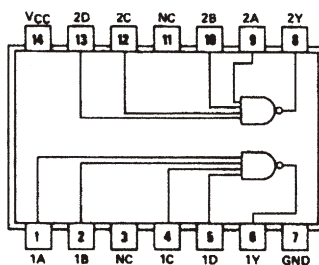
TTL Logic Diagrams (cont'd)

Diag. 116 16-Pin DIP See Fig. D8
ECG74HC139, ECG74LS139



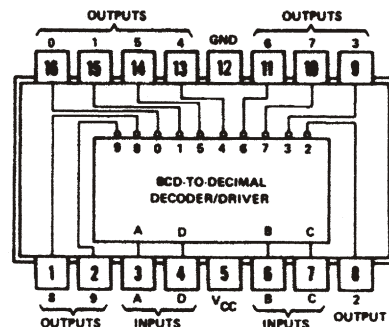
Dual 2-Line-to-4-Line Decoder/Demultiplexer

Diag. 117 14-Pin DIP See Fig. D6
ECG74S140



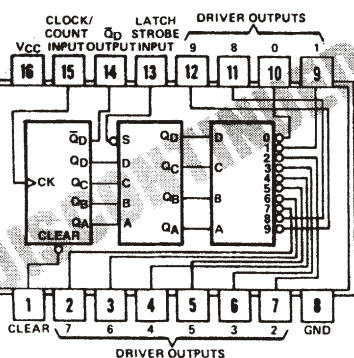
Dual 4-Input NAND 50 Ohm Line Driver

Diag. 118 16-Pin DIP See Fig. D8
ECG74141



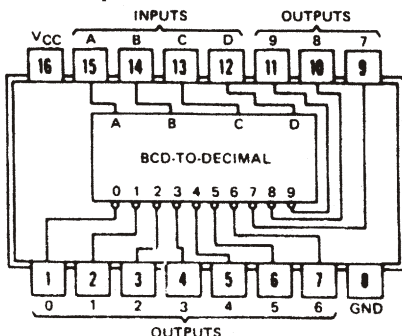
BCD-to-Decimal Decoder/Driver for Cold Cathode Tubes

Diag. 119 16-Pin DIP See Fig. D8
ECG74142



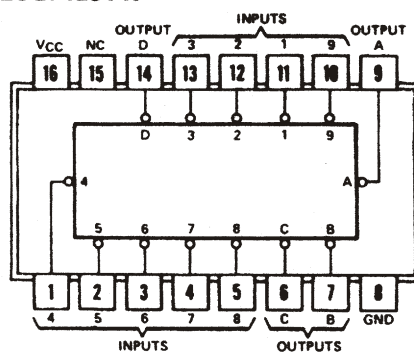
BCD Counter/4-Bit Latch/BCD Decoder/Driver

Diag. 122 16-Pin DIP See Fig. D8
ECG74145, ECG74LS145



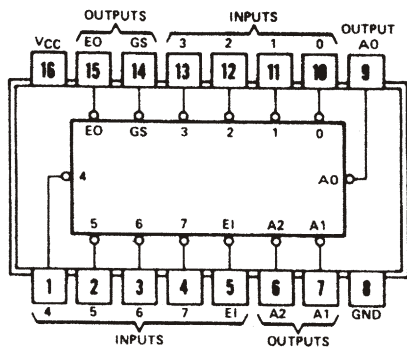
BCD-to-Decimal Decoder Driver with Open Collector Output

Diag. 123 16-Pin DIP See Fig. D8
ECG74LS147



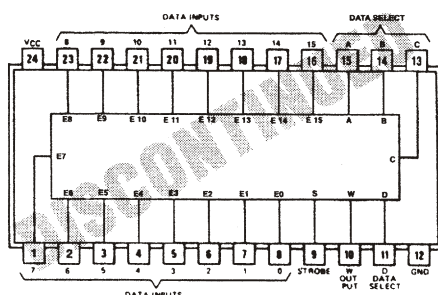
Decimal-to-BCD-Priority Encoder

Diag. 124 16-Pin DIP See Fig. D8
ECG74LS148



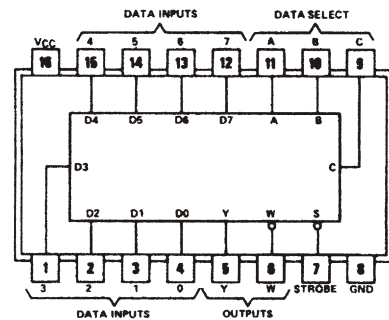
8-Line-to-3-Line Octal Priority Encoder

Diag. 125 24-Pin DIP See Fig. D15
ECG74150



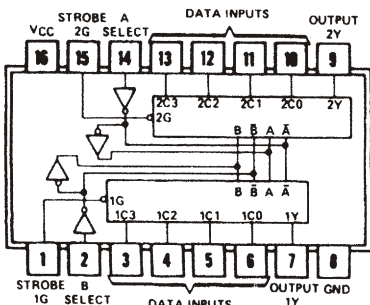
16-Line-to-1-Line Data Selector/Multiplexer

Diag. 126 16-Pin DIP See Fig. D8
ECG74151*, ECG74C151, ECG74HC151, ECG74LS151



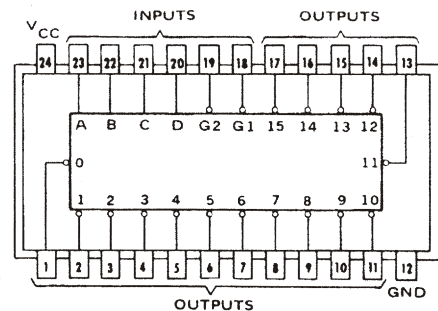
8-Line-to-1-Line Data Selector/Multiplexer with Strobe * DISCONTINUED

Diag. 128 16-Pin DIP See Fig. D8
ECG74153, ECG74HC153, ECG74LS153



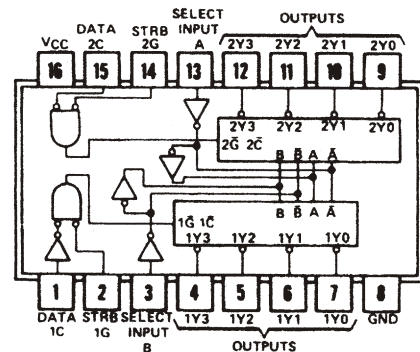
Dual 4-Line-to-1-Line Data Selector/Multiplexer

Diag. 129 24-Pin DIP See Fig. D15
ECG74154, ECG74C154*, ECG74HC154



4-Line-to-16-Line Decoder/Demultiplexer * DISCONTINUED

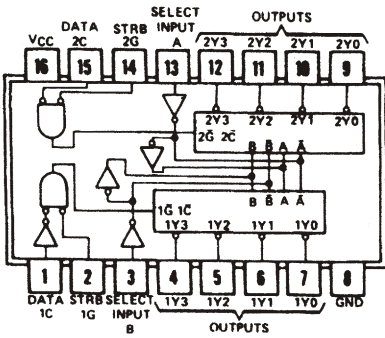
Diag. 130 16-Pin DIP See Fig. D8
ECG74155, ECG74LS155



Dual 1-Line-to-4-Line Decoder/Demultiplexer

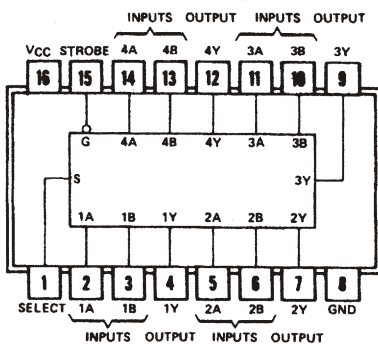
TTL Logic Diagrams (cont'd)

Diag. 131 16-Pin DIP See Fig. D8
ECG74156, ECG74LS156



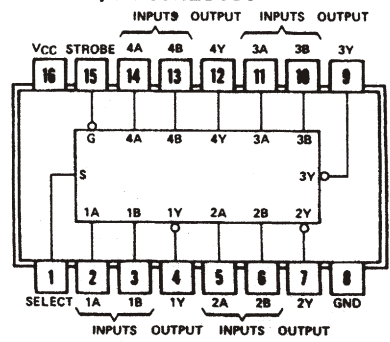
Dual 1-Line-to-4-Line Decoder/Demultiplexer with Open Collector Output

Diag. 132 16-Pin DIP See Fig. D8
ECG74157, ECG74C157, ECG72LS157,



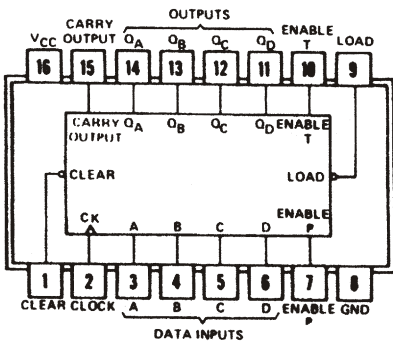
Quad 2-Line-to-1-Line Data Selector/Multiplexer with Non-Inverting Output

Diag. 133 16-Pin DIP See Fig. D8
ECG74158, ECG72LS158



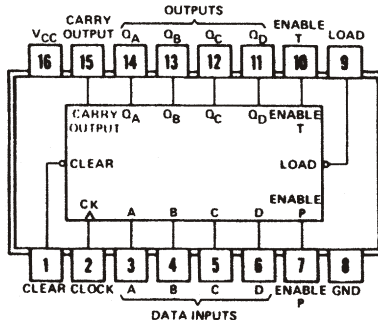
Quad 2-Line-to-1-Line Data Selector/Multiplexer with Inverting Output

Diag. 134 16-Pin DIP See Fig. D8
ECG74160, ECG74LS160A



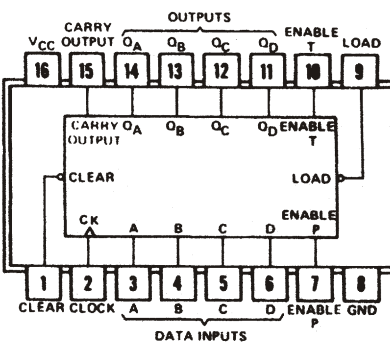
Presettable Synchronous Decade Counter with Direct Clear

Diag. 135 16-Pin DIP See Fig. D8
ECG74161, ECG74C161, ECG74HC161, ECG74HCT161, ECG74LS161A



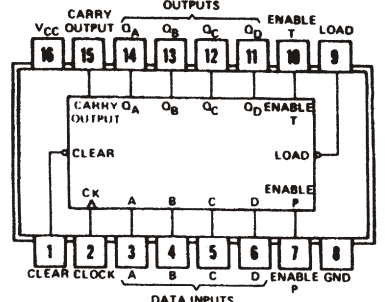
Presettable Synchronous 4-Bit Binary Counter with Direct Clear

Diag. 136 16-Pin DIP See Fig. D8
ECG74162, ECG74LS162A



Presettable Synchronous Decade Counter with Synchronous Clear

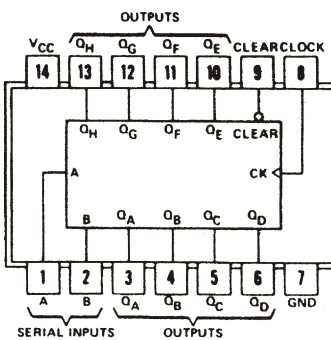
Diag. 137 16-Pin DIP See Fig. D8
ECG74163*, ECG74HC163, ECG74HCT163, ECG74LS163A



Presettable Synchronous 4-Bit Binary Counter with Synchronous Clear

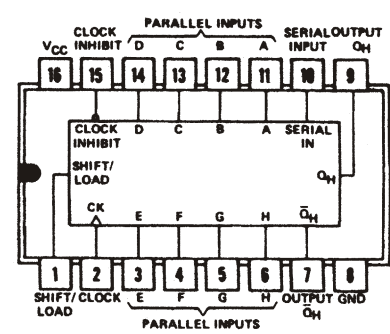
* DISCONTINUED

Diag. 138 14-Pin DIP See Fig. D6
ECG74164, ECG74C164, ECG74HC164, ECG74LS164



8-Bit Serial-In/Parallel-Out Shift Register

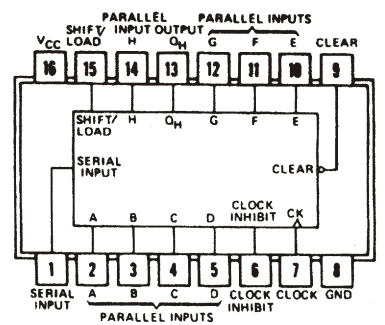
Diag. 139 16-Pin DIP See Fig. D8
ECG74165, ECG74HC165, ECG74LS165*



8-Bit Parallel-In/Serial-Out Shift Register

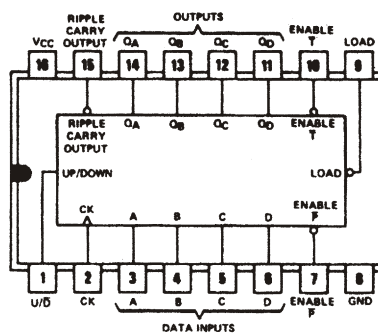
* DISCONTINUED

Diag. 140 16-Pin DIP See Fig. D8
ECG74166, ECG74LS166



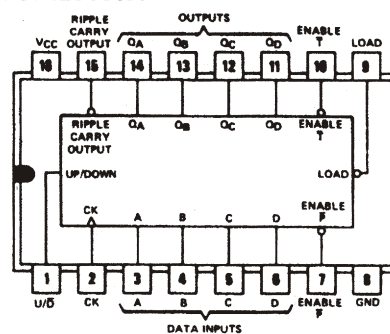
8-Bit Serial or Parallel-In/Serial-Out Shift Register

Diag. 141 16-Pin DIP See Fig. D8
ECG74LS168A



Presettable Synchronous Decade Up/Down Counter

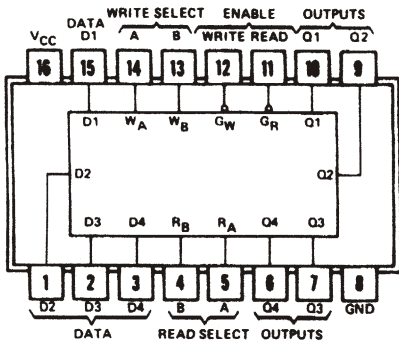
Diag. 142 16-Pin DIP See Fig. D8
ECG74LS169A



Presettable Synchronous 4-Bit Binary Up/Down Counter

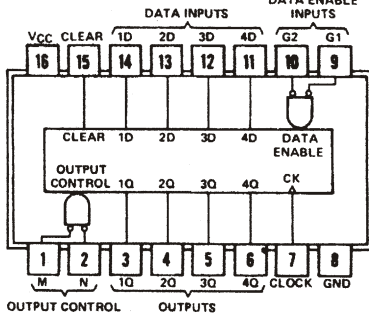
TTL Logic Diagrams (cont'd)

Diag. 143 16-Pin DIP See Fig. D8
ECG74170, ECG74LS170



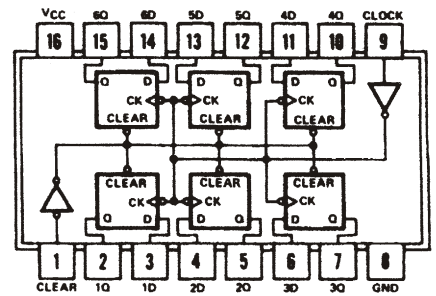
4 x 4 Register File with Open Collector Output

Diag. 144 16-Pin DIP See Fig. D8
ECG74173*, ECG74C173, ECG74HC173,
ECG74LS173



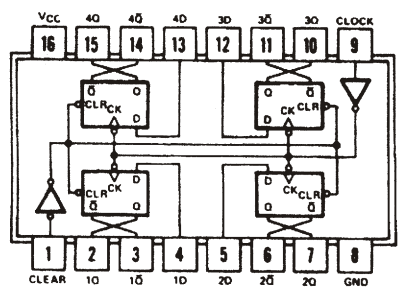
4-Bit "D" Register with 3-State Output
* DISCONTINUED

Diag. 145 16-Pin DIP See Fig. D8
ECG74174, ECG74C174, ECG74HC174,
ECG74HCT174, ECG74LS174,
ECG74S174



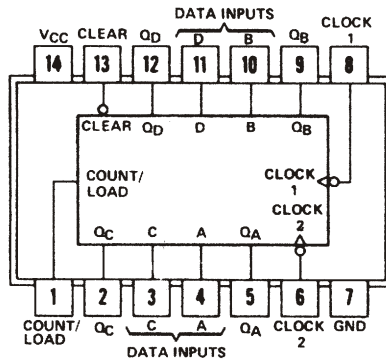
Hex "D" Flip-Flop with Clear

Diag. 146 16-Pin DIP See Fig. D8
ECG74175, ECG74C175, ECG74HC175,
ECG74LS175, ECG74S175*



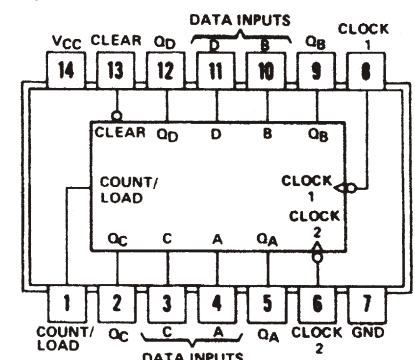
Quad "D" Flip-Flop with Complementary Outputs
* DISCONTINUED

Diag. 147 14-Pin DIP See Fig. D6
ECG74176



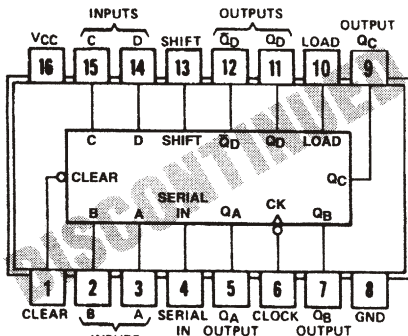
Presettable Decade Counter/Latch

Diag. 148 14-Pin DIP See Fig. D6
ECG74177



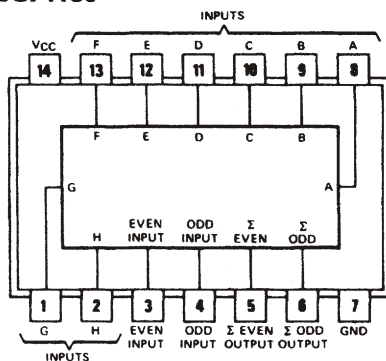
Presettable 4-Bit Binary Counter/Latch

Diag. 150 16-Pin DIP See Fig. D8
ECG74179



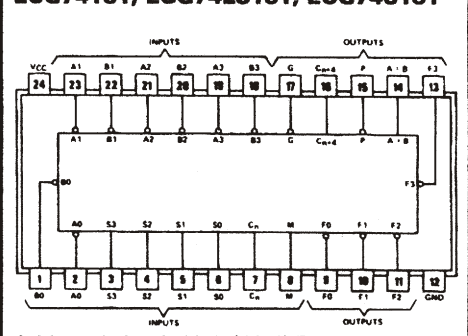
4-Bit Parallel Shift Register with Complementary Final Stage

Diag. 151 14-Pin DIP See Fig. D6
ECG74180



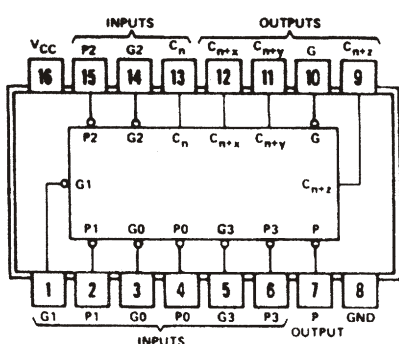
9-Bit Odd/Even Parity Generator/Checker

Diag. 152 24-Pin DIP See Fig. D15
ECG74181, ECG74LS181, ECG74S181*



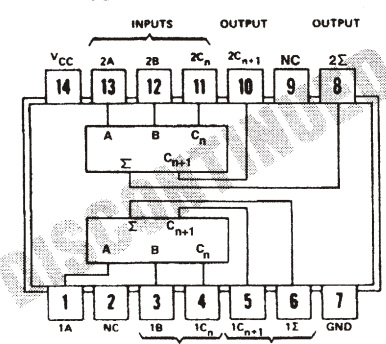
Arithmetic Logic Unit (ALU)/Function Generator
* DISCONTINUED

Diag. 153 16-Pin DIP See Fig. D8
ECG74182



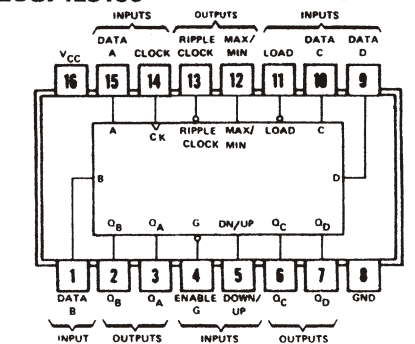
Look-Ahead Carry Generator

Diag. 154 14-Pin DIP See Fig. D6
ECG74H183



Dual Carry/Save Adder

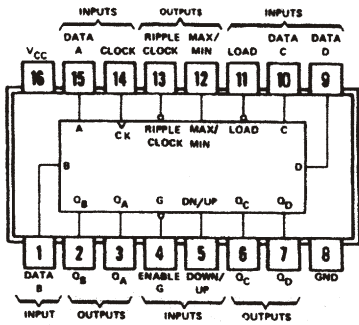
Diag. 155 16-Pin DIP See Fig. D8
ECG74LS190



Presettable Synchronous Decade Up/Down Counter

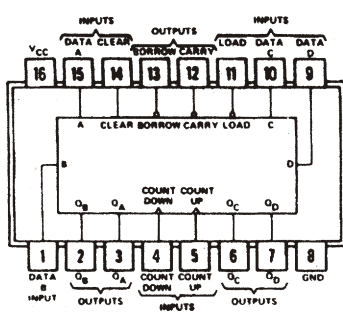
TTL Logic Diagrams (cont'd)

Diag. 156 16-Pin DIP See Fig. D8
ECG74191, ECG74LS191*



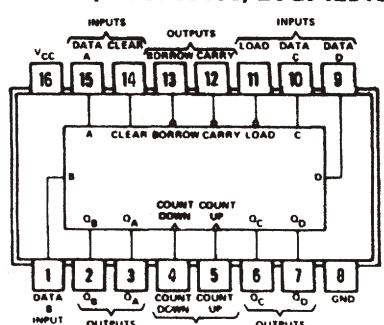
Presettable Synchronous 4-Bit Binary Up/Down Counter * DISCONTINUED

Diag. 157 16-Pin DIP See Fig. D8
ECG74192*, ECG74C192, ECG74LS192



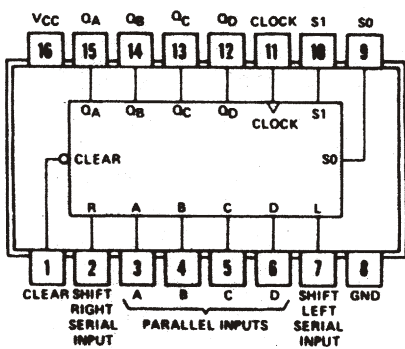
Presettable Synchronous Decade Up/Down Counter with Dual Clocks * DISCONTINUED

Diag. 158 16-Pin DIP See Fig. D8
ECG74193, ECG74C193, ECG74LS193



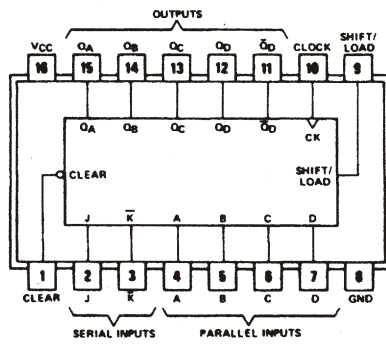
Presettable Synchronous 4-Bit Binary Up/Down Counter with Dual Clocks

Diag. 159 16-Pin DIP See Fig. D8
ECG74LS194A, ECG74S194



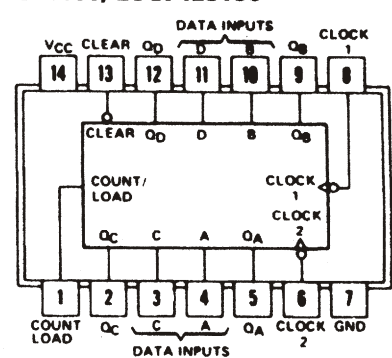
4-Bit Bidirectional Parallel Shift Register

Diag. 160 16-Pin DIP See Fig. D8
ECG74195, ECG74LS195A



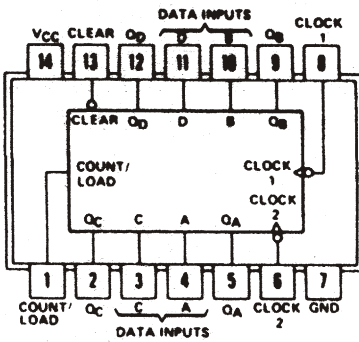
4-Bit Parallel Shift Register with Complementary Final Stage

Diag. 161 14-Pin DIP See Fig. D6
ECG74196, ECG74LS196



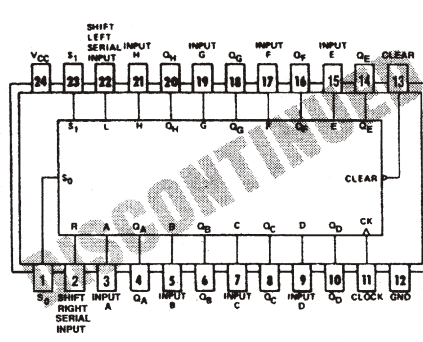
Presettable Decade Counter/Latch

Diag. 162 14-Pin DIP See Fig. D6
ECG74197*, ECG74LS197



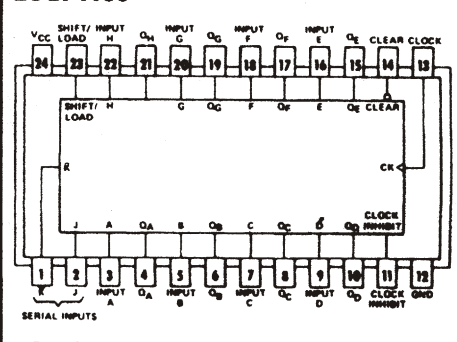
Presettable 4-Bit Binary Counter/Latch * DISCONTINUED

Diag. 163 24-Pin DIP See Fig. D15
ECG74198



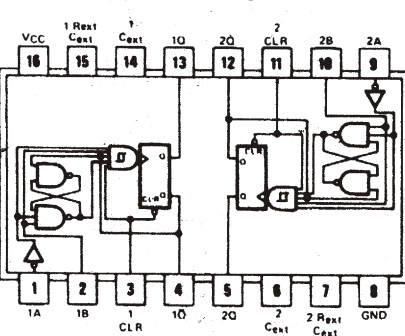
8-Bit Bidirectional Parallel Shift Register

Diag. 164 24-Pin DIP See Fig. D15
ECG74199



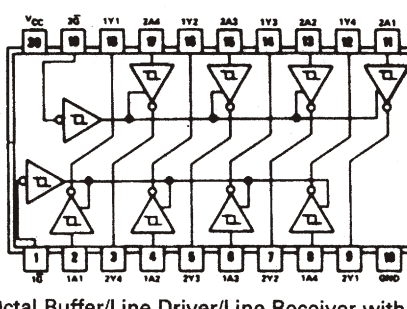
8-Bit Serial or Parallel-In/Parallel-Out Shift Register

Diag. 165 16-Pin DIP See Fig. D8
ECG74221, ECG74C221, ECG74LS221



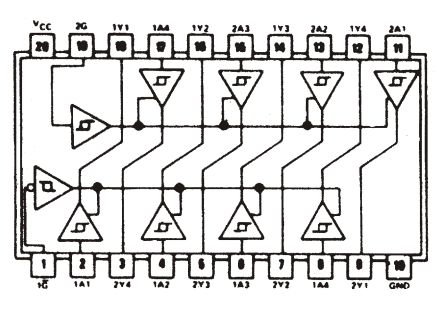
Dual Monostable Multivibrator

Diag. 166 20-Pin DIP See Fig. D12
ECG74C240, ECG74HC240,
ECG74HCT240*, ECG74LS240



Octal Buffer/Line Driver/Line Receiver with Inverting 3-State Output * DISCONTINUED

Diag. 167 20-Pin DIP See Fig. D12
ECG74LS241



Octal Buffer/Line Driver/Line Receiver with Non-Inverting 3-State Output

TTL Logic Diagrams (cont'd)

Diag. 168 14-Pin DIP See Fig. D6
ECG74LS242

Quad Bus Transceiver with Inverting 3-State Output

Diag. 169 14-Pin DIP See Fig. D6
ECG74LS243

Quad Bus Transceiver with Non-Inverting 3-State Output

Diag. 170 20-Pin DIP See Fig. D12
ECG74C244, ECG74HC244, ECG74HCT244, ECG74LS244

Octal Buffer/Line Driver/Line Receiver with Non-Inverting 3-State Output

Diag. 171 20-Pin DIP See Fig. D12
ECG74LS245

Octal Bus Transceiver with Non-Inverting 3-State Output

Diag. 172 16-Pin DIP See Fig. D8
ECG74LS247

BCD-to-7-Segment Decoder/Driver with Hi-Volt (15 V) Open Collector Output

Diag. 173 16-Pin DIP See Fig. D8
ECG74LS248

BCD-to-7-Segment Decoder/Driver

Diag. 174 16-Pin DIP See Fig. D8
ECG74249, ECG74LS249

BCD-to-7-Segment Decoder/Driver with Open Collector Output

Diag. 175 16-Pin DIP See Fig. D8
ECG74251, ECG74LS251, ECG74S251

8-Line-to-1-Line Data Selector/Multiplexer with Complementary 3-State Output

Diag. 176 16-Pin DIP See Fig. D8
ECG74LS253

Dual 4-Line-to-1-Line Data Selector/Multiplexer with 3-State Output

Diag. 177 16-Pin DIP See Fig. D8
ECG74HC257, ECG74LS257

Quad 2-Line-to-1-Line Data Selector/Multiplexer with 3-State Output

Diag. 178 16-Pin DIP See Fig. D8
ECG74LS258, ECG74S258

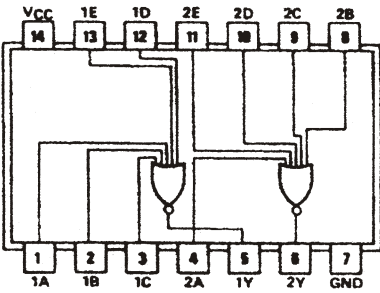
Quad 2-Line-to-1-Line Data Selector/Multiplexer with Inverting 3-State Output

Diag. 179 16-Pin DIP See Fig. D8
ECG74HC259, ECG74LS259

8-Bit Addressable Latch

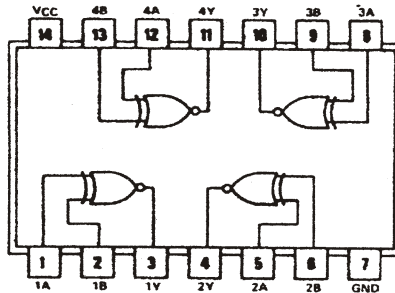
TTL Logic Diagrams (cont'd)

Diag. 180 14-Pin DIP See Fig. D6
ECG74LS260



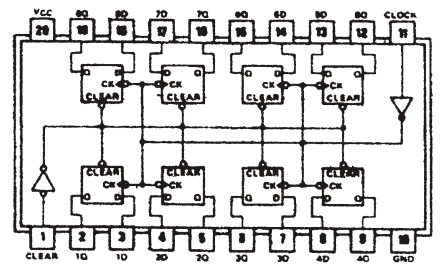
Dual 5-Input NOR Gate

Diag. 181 14-Pin DIP See Fig. D6
ECG74LS266



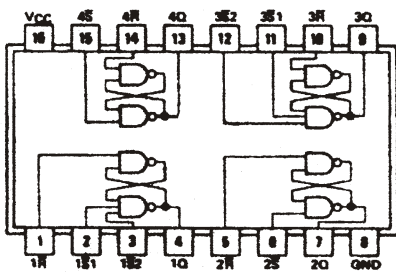
Quad Exclusive NOR Gate with Open Collector Output

Diag. 182 20-Pin DIP See Fig. D12
ECG74HC273, ECG74HCT273,
ECG74LS273



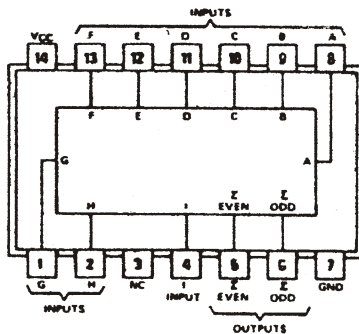
Octal "D" Flip-Flop with Clear

Diag. 183 16-Pin DIP See Fig. D8
ECG74LS279



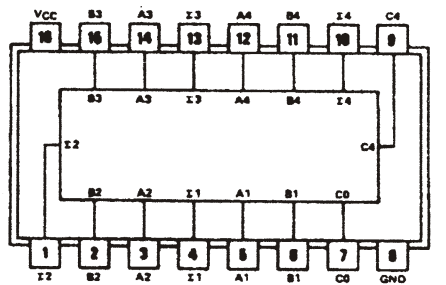
Quad S-R Latch

Diag. 184 14-Pin DIP See Fig. D6
ECG74LS280



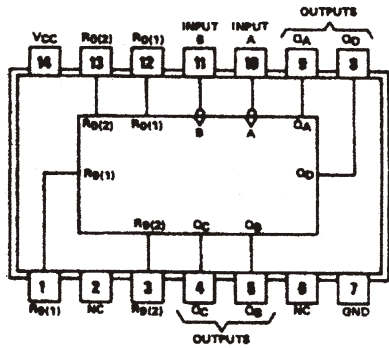
9-Bit Odd/Even Parity Generator/Checker

Diag. 185 16-Pin DIP See Fig. D8
ECG74LS283



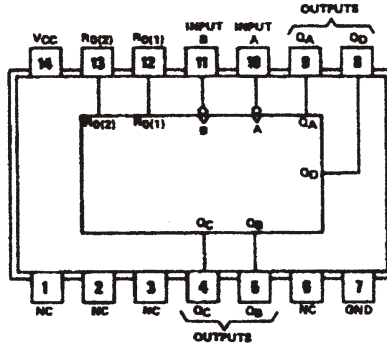
4-Bit Full Adder

Diag. 186 14-Pin DIP See Fig. D6
ECG74290, ECG74LS290



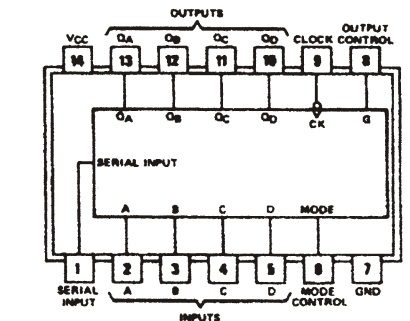
Decade Counter

Diag. 187 14-Pin DIP See Fig. D6
ECG74LS293



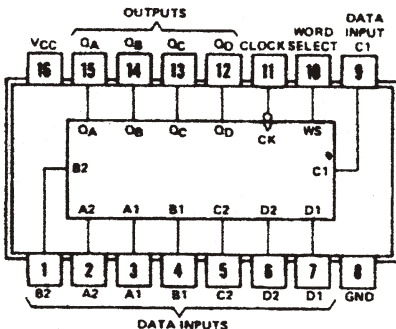
4-Bit Binary Counter

Diag. 188 14-Pin DIP See Fig. D6
ECG74LS295A



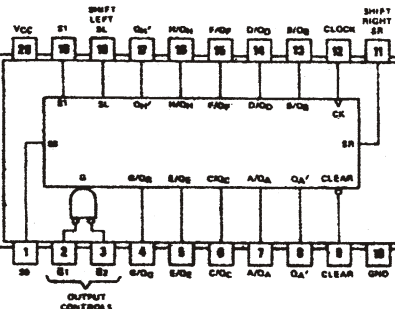
4-Bit Bidirectional Parallel Shift Register with 3-State Output

Diag. 189 16-Pin DIP See Fig. D8
ECG74LS298



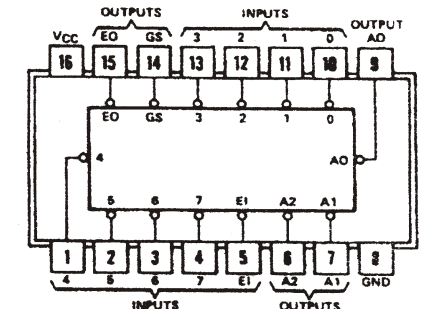
Quad 2-Input Multiplexer with Storage

Diag. 190 20-Pin DIP See Fig. D12
ECG74HC299, ECG74LS299



8-Bit Bidirectional Shift/Storage Register with 3-State Output

Diag. 191 16-Pin DIP See Fig. D8
ECG74LS348



8-Line-to-3-Line Priority Encoder with 3-State Output

TTL Logic Diagrams (cont'd)

Diag. 192 16-Pin DIP See Fig. D8
ECG74LS352

Dual 4-Line-to-1-Line Data Selector/
 Multiplexer with 3-State Output

Diag. 193 16-Pin DIP See Fig. D8
ECG74LS353

Dual 4-Line-to-1-Line Data Selector/
 Multiplexer with Inverting 3-State Output

Diag. 194 20-Pin DIP See Fig. D12
ECG74LS363

Octal "D" Transparent Latch with 3-State
 Output

Diag. 195 20-Pin DIP See Fig. D12
ECG74LS364

Octal "D" Flip-Flop with 3-State Output

Diag. 196 16-Pin DIP See Fig. D8
ECG74365, ECG74LS365A

Hex Bus Driver with Non-Inverting 3-State
 Output (Common Enable)

Diag. 197 16-Pin DIP See Fig. D8
ECG74366, ECG74LS366A

Hex Bus Driver with Inverting 3-State
 Output (Common Enable)

Diag. 198 16-Pin DIP See Fig. D8
ECG74367, ECG74LS367

Hex Bus Driver with Non-Inverting 3-State
 Output (4-Line/2-Line Enable)

Diag. 199 16-Pin DIP See Fig. D8
ECG74368, ECG74LS368

Hex Bus Driver with Inverting 3-State
 Output (4-Line/2-Line Enable)

Diag. 200 20-Pin DIP See Fig. D12
**ECG74C373, ECG74HC373,
 ECG74HCT373, ECG74HC573,
 ECG74HCT573, ECG74LS373**

Octal "D" Transparent Latch with 3-State
 Output

Diag. 201 20-Pin DIP See Fig. D12
**ECG74C374, ECG74HC374,
 ECG74HCT374, ECG74HC574,
 ECG74HCT574*, ECG74LS374**

Octal "D" Flip-Flop with 3-State Output
 * DISCONTINUED

Diag. 202 20-Pin DIP See Fig. D12
ECG74HC377, ECG74LS377*

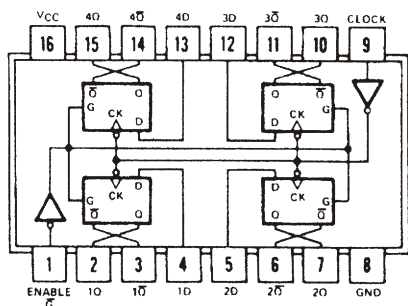
Octal "D" Flip-Flop with Common Enable
 * DISCONTINUED

Diag. 203 16-Pin DIP See Fig. D8
ECG74LS378

Hex "D" Flip-Flop with Common Enable

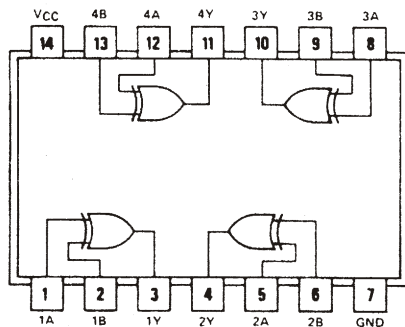
TTL Logic Diagrams (cont'd)

Diag. 204 16-Pin DIP See Fig. D8
ECG74LS379



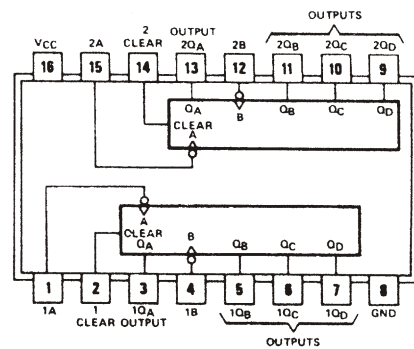
Quad "D" Flip-Flop with Complementary Outputs

Diag. 205 14-Pin DIP See Fig. D6
ECG74LS386



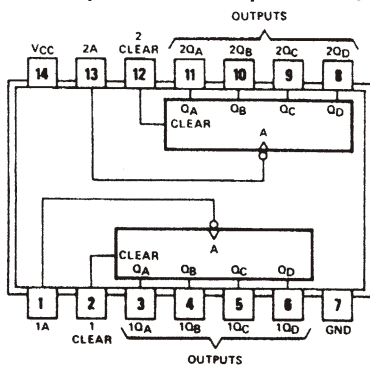
Quad Exclusive OR Gate

Diag. 206 16-Pin DIP See Fig. D8
ECG74HC390, ECG74LS390



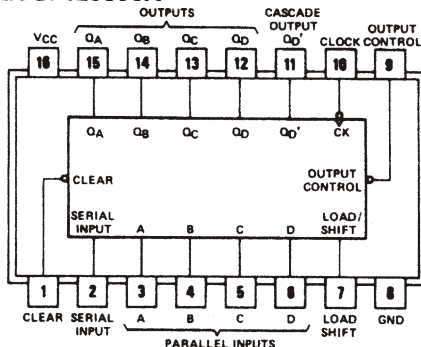
Dual Decade Counter

Diag. 207 14-Pin DIP See Fig. D6
ECG74393, ECG74HC393, ECG74LS393



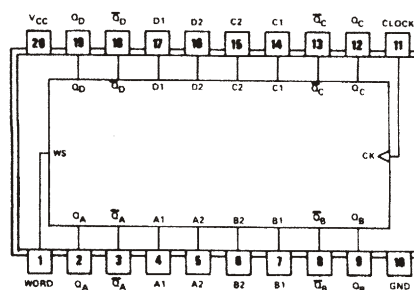
Dual 4-Bit Binary Counter

Diag. 208 16-Pin DIP See Fig. D8
ECG74LS395A



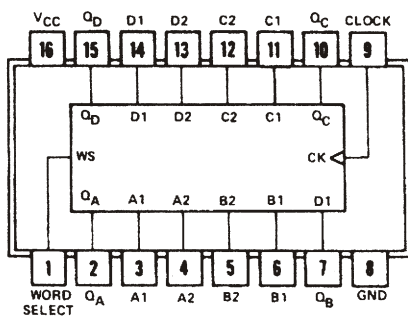
4-Bit Cascadable Parallel Shift Register with 3-State Output

Diag. 209 20-Pin DIP See Fig. D12
ECG74LS398



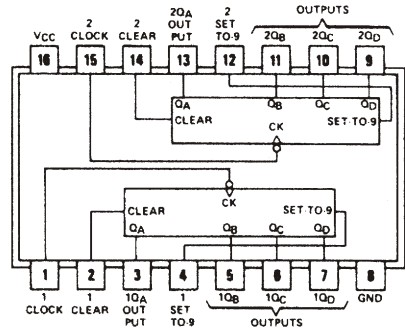
Quad 2-Input Multiplexer with Storage Complementary Outputs

Diag. 210 16-Pin DIP See Fig. D8
ECG74LS399



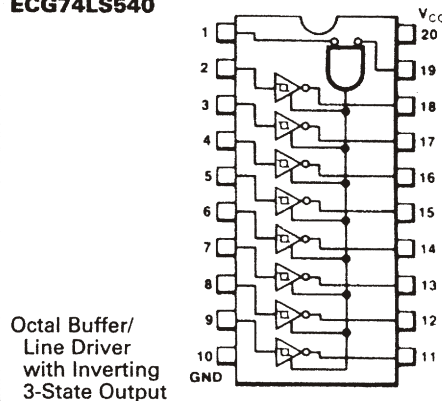
Quad 2-Input Multiplexer with Storage

Diag. 211 16-Pin DIP See Fig. D8
ECG74490, ECG74LS490



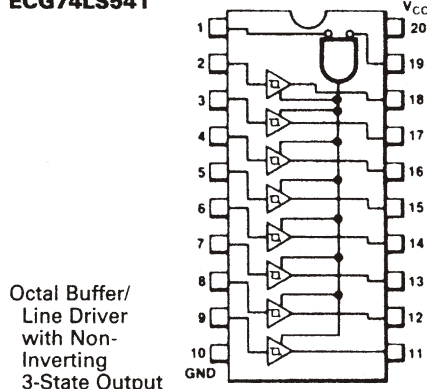
Dual Decade Counter

Diag. 212 20-Pin DIP See Fig. D12
ECG74LS540



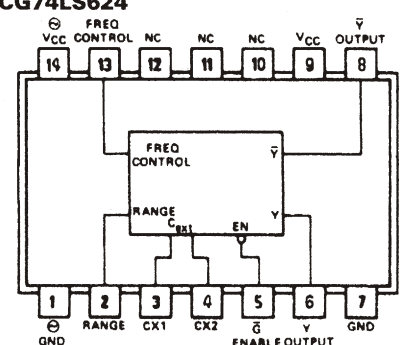
Octal Buffer/Line Driver with Inverting 3-State Output

Diag. 213 20-Pin DIP See Fig. D12
ECG74LS541



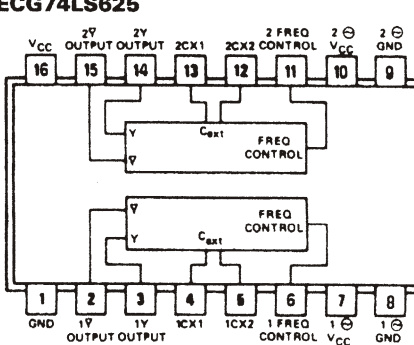
Octal Buffer/Line Driver with Non-Inverting 3-State Output

Diag. 214 14-Pin DIP See Fig. D6
ECG74LS624



Voltage Controlled Oscillator with Complementary Output

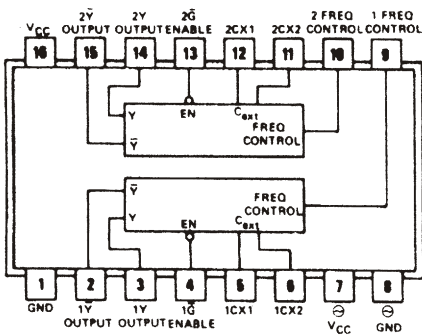
Diag. 215 16-Pin DIP See Fig. D8
ECG74LS625



Dual Voltage Controlled Oscillator with Complementary Output

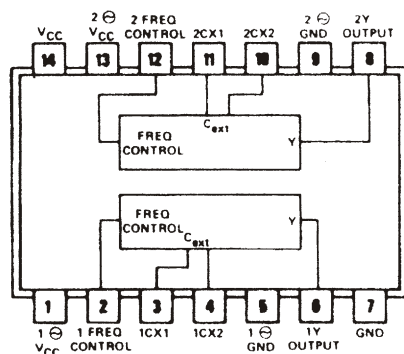
TTL Logic Diagrams (cont'd)

Diag. 216 16-Pin DIP See Fig. D8
ECG74LS626



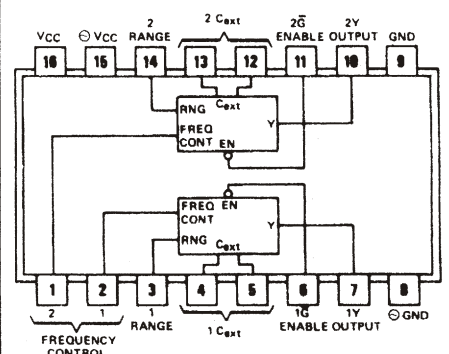
Dual Voltage Controlled Oscillator with Complementary Output and Enable

Diag. 217 14-Pin DIP See Fig. D6
ECG74LS627



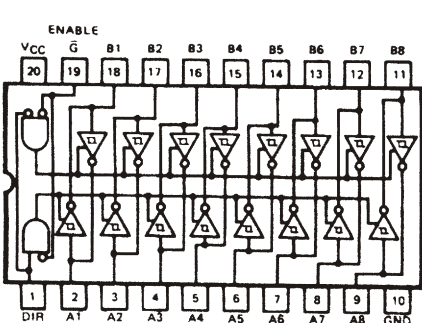
Dual Voltage Controlled Oscillator

Diag. 218 16-Pin DIP See Fig. D8
ECG74LS629



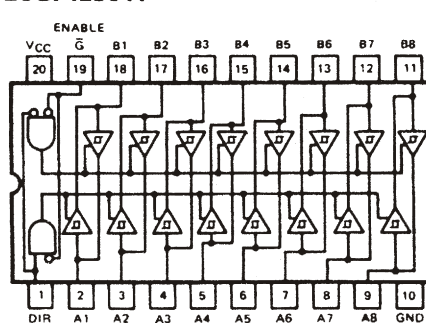
Dual Voltage Controlled Oscillator with Enable

Diag. 219 20-Pin DIP See Fig. D12
ECG74LS640



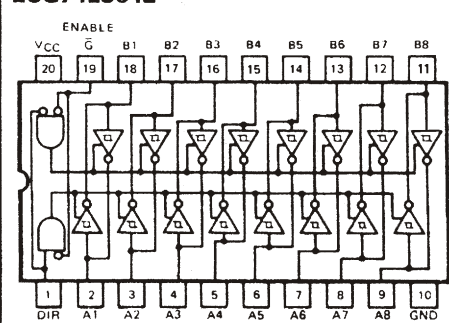
Octal Bus Transceiver with Inverting 3-State Output

Diag. 220 20-Pin DIP See Fig. D12
ECG74LS641



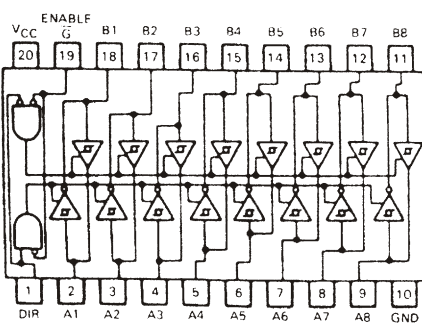
Octal Bus Transceiver with Non-Inverting 3-State Open Collector Output

Diag. 221 20-Pin DIP See Fig. D12
ECG74LS642



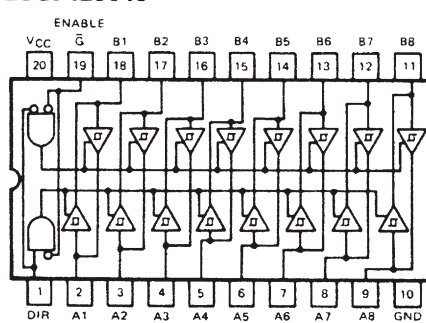
Octal Bus Transceiver with Inverting Open Collector Output

Diag. 222 20-Pin DIP See Fig. D12
ECG74LS643



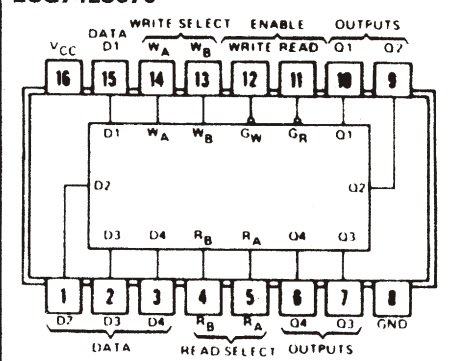
Octal Bus Transceiver with Inverting and Non-Inverting 3-State Output

Diag. 223 20-Pin DIP See Fig. D12
ECG74LS645



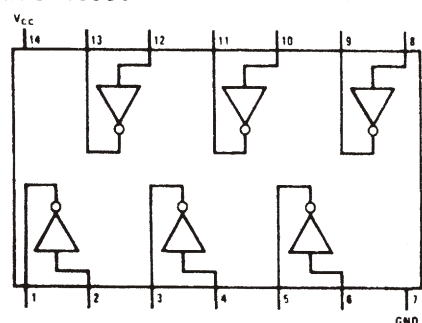
Octal Bus Transceiver with Non-Inverting 3-State Output

Diag. 224 16-Pin DIP See Fig. D8
ECG74LS670



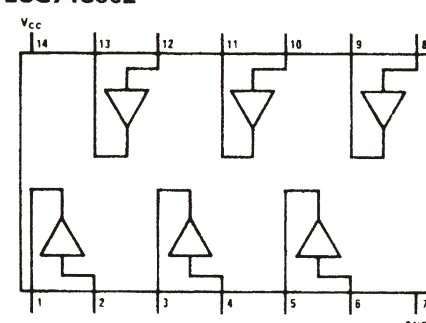
4 x 4 Register File with 3-State Output

Diag. 225 14-Pin DIP See Fig. D6
ECG74C901



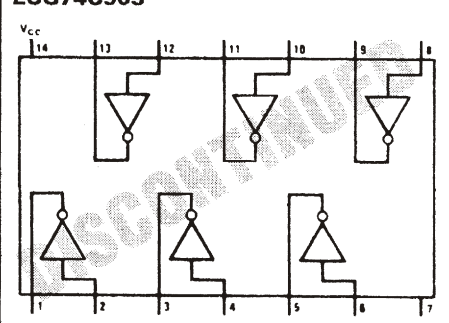
Hex CMOS to TTL Interface Buffer (Inverting Output)

Diag. 226 14-Pin DIP See Fig. D6
ECG74C902



Hex CMOS to TTL Interface Buffer (Non-Inverting Output)

Diag. 227 14-Pin DIP See Fig. D6
ECG74C903

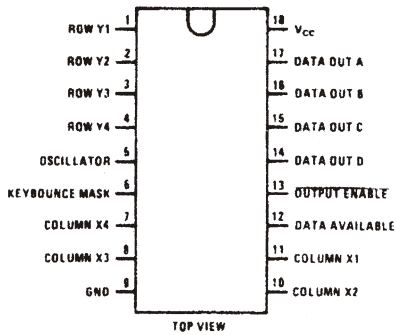


Hex PMOS to TTL/CMOS Interface Buffer (Inverting Output)

TTL Logic Diagrams (cont'd)

Diag. 229 18-Pin DIP See Fig. D10

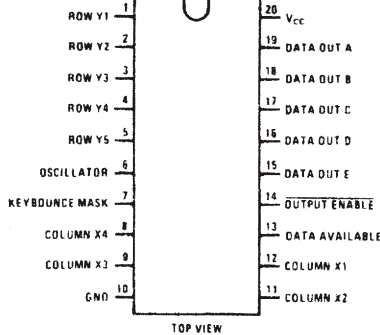
ECG74C922



16-Key Keyboard Encoder with 3-State Output

Diag. 230 20-Pin DIP See Fig. D12

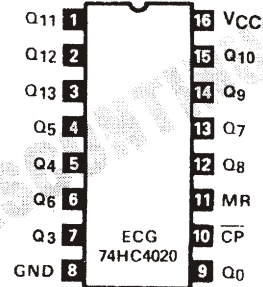
ECG74C923



20-Key Keyboard Encoder with 3-State Output

Diag. 232 16-Pin DIP See Fig. D8

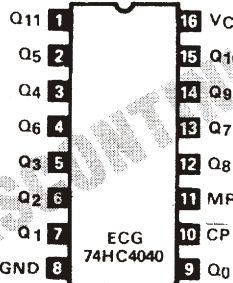
ECG74HC4020



14-Stage Binary/Ripple Counter

Diag. 233 16-Pin DIP See Fig. D8

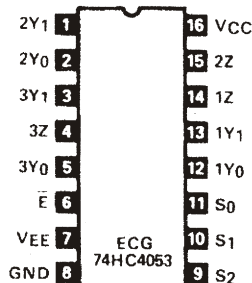
ECG74HC4040



12-Stage Binary/Ripple Counter

Diag. 234 16-Pin DIP See Fig. D8

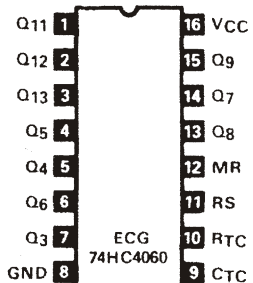
ECG74HC4053



Triple 2-Channel Analog Multiplexer

Diag. 235 16-Pin DIP See Fig. D8

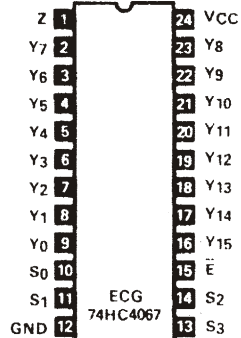
ECG74HC4060



14-Stage Ripple-Carry Binary Counter/Divider and Oscillator

Diag. 236 24-Pin DIP See Fig. D15

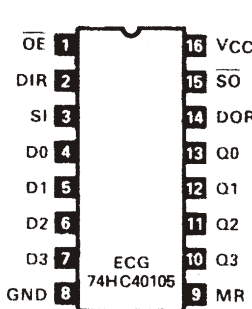
ECG74HC4067



16-Channel Multiplexer/Demultiplexer

Diag. 237 16-Pin DIP See Fig. D8

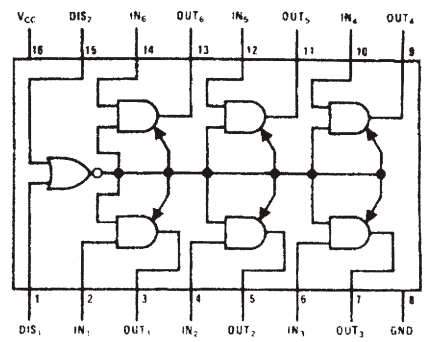
ECG74HC40105



4-Bit x 16-Word FIFO Register

Diag. 238 16-Pin DIP See Fig. D8

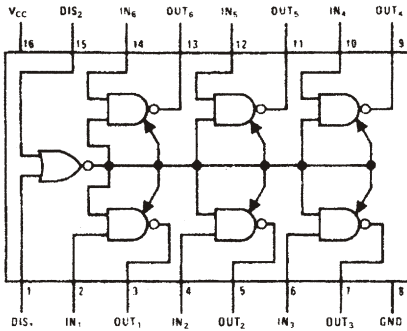
ECG80C95



Hex Buffer with 3-State Output (Common Enable)

Diag. 239 16-Pin DIP See Fig. D8

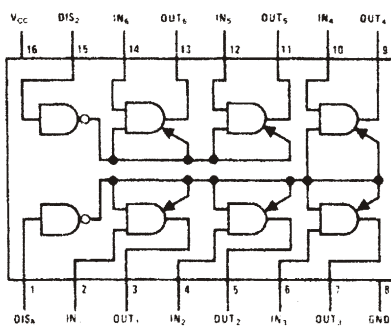
ECG80C96



Hex Inverter/Buffer with 3-State Output (Common Enable)

Diag. 240 16-Pin DIP See Fig. D8

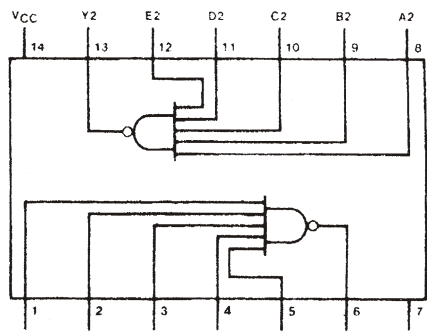
ECG80C97



Hex Buffer with 3-State Output (2-Line/4-Line Enable)

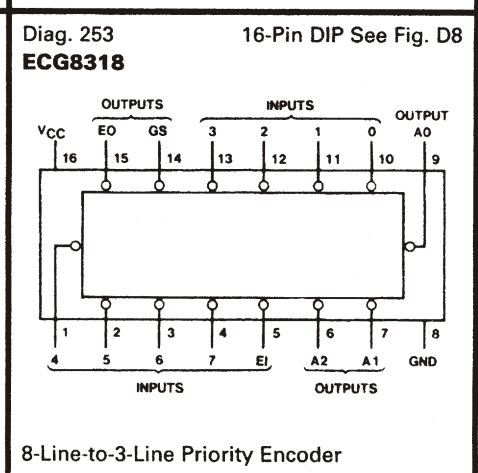
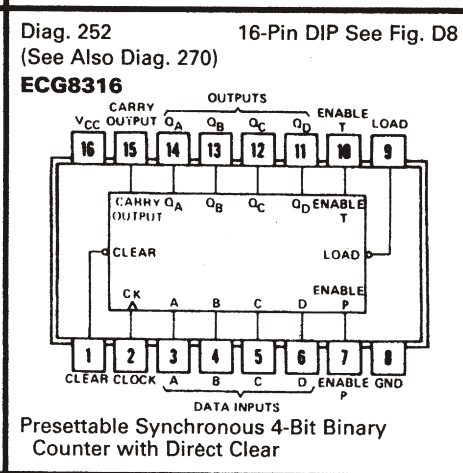
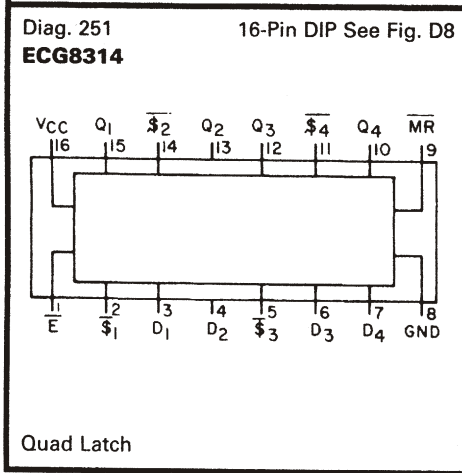
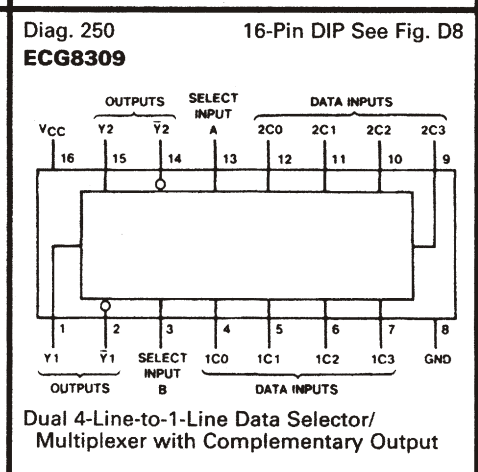
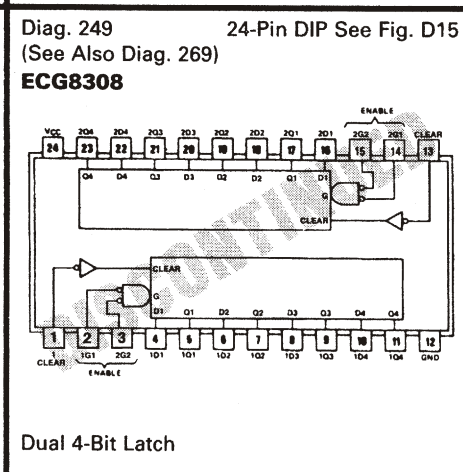
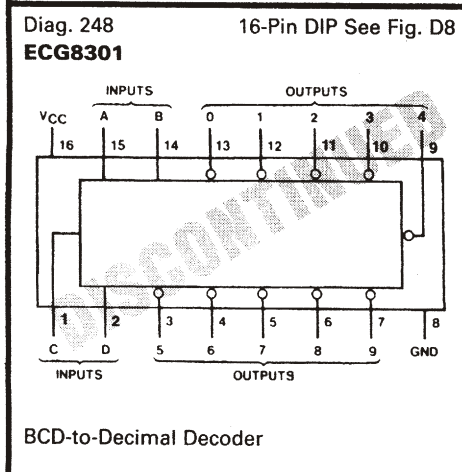
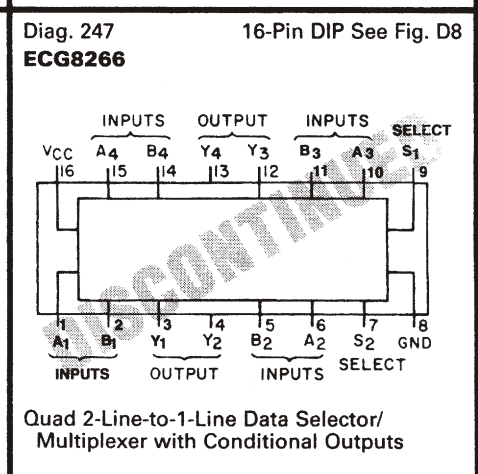
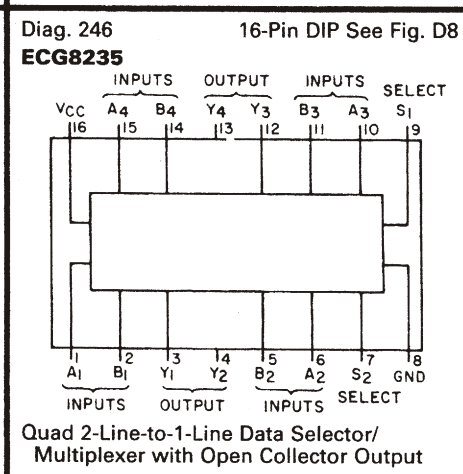
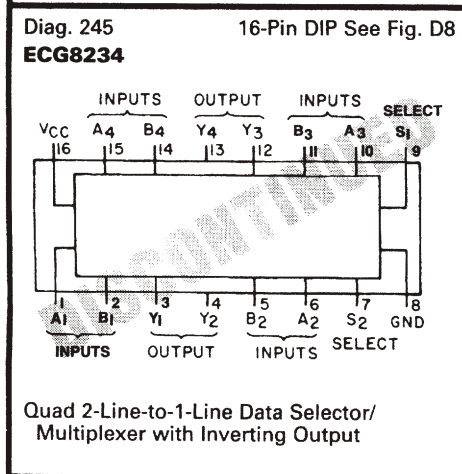
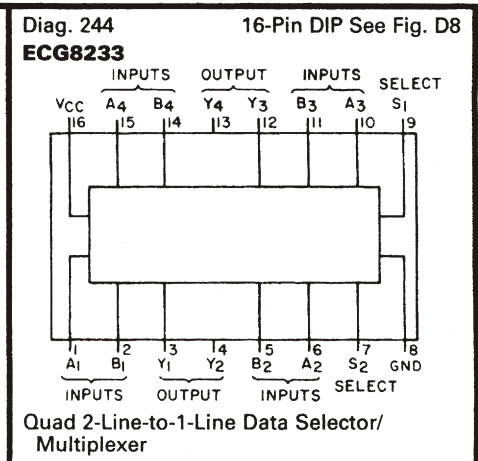
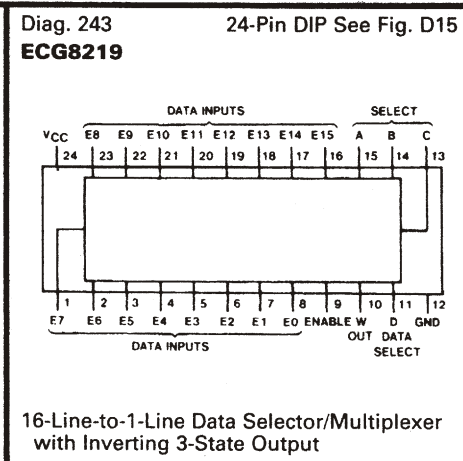
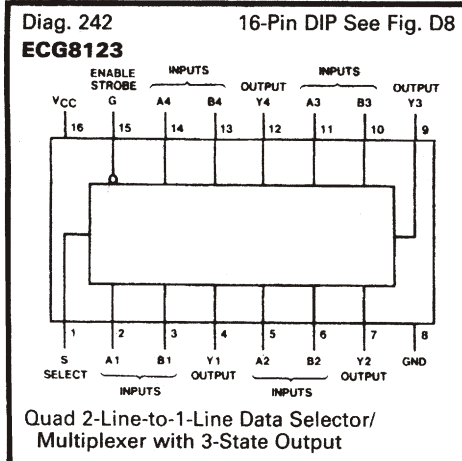
Diag. 241 14-Pin DIP See Fig. D6

ECG8092



Dual 5-Input NAND Gate

TTL Logic Diagrams (cont'd)

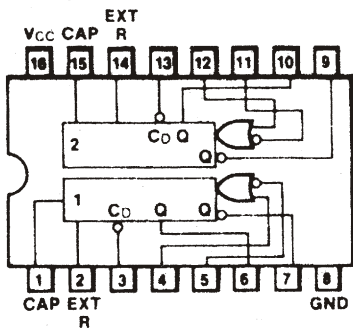


TTL Logic Diagrams (cont'd)

<p>Diag. 254 ECG8321 16-Pin DIP See Fig. D8</p> <p>Dual 2-Line-to-4-Line Decoder/Demultiplexer</p>	<p>Diag. 255 ECG8328 16-Pin DIP See Fig. D8</p> <p>Dual 8-Bit Serial Shift Register</p>	<p>Diag. 257 ECG8370 16-Pin DIP See Fig. D8</p> <p>Hexadecimal-to-7-Segment Decoder/Latch/Driver with Open Collector Output</p>
<p>Diag. 258 ECG8374 16-Pin DIP See Fig. D8</p> <p>Hexadecimal-to-7-Segment Decoder/Driver/Latch for Common Anode Displays</p>	<p>Diag. 259 ECG8520 16-Pin DIP See Fig. D8</p> <p>Module "N" Divider</p>	<p>Diag. 260 ECG8542 16-Pin DIP See Fig. D8</p> <p>Quad I/O Register with 3-State Output</p>
<p>Diag. 261 ECG8546 16-Pin DIP See Fig. D8</p> <p>8-Bit Bidirectional I/O Shift Register with 3-State I/O Lines</p>	<p>Diag. 263 ECG8553 16-Pin DIP See Fig. D8</p> <p>8-Bit Latch with 3-State I/O Lines</p>	<p>Diag. 264 ECG8554 16-Pin DIP See Fig. D8</p> <p>Synchronous 4-Bit Binary Counter/Latch with 3-State Output</p>
<p>Diag. 266 ECG8556 16-Pin DIP See Fig. D8</p> <p>Presettable Synchronous 4-Bit Binary Counter with 3-State Output</p>	<p>Diag. 267 ECG8613 16-Pin DIP See Fig. D8</p> <p>Quad Gated "D" Flip-Flop</p>	<p>Diag. 268 ECG8853 16-Pin DIP See Fig. D8</p> <p>Dual Retriggerable/Resettable Monostable Multivibrator with Delay</p>

TTL Logic Diagrams (cont'd)

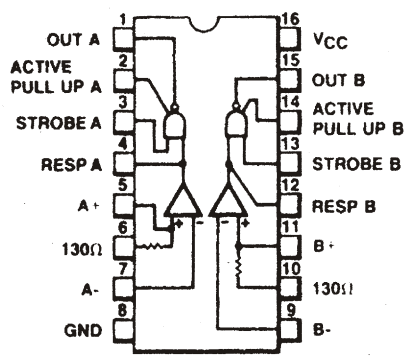
Diag. 273 16-Pin DIP See Fig. D8
ECG9602, ECG96L02* ECG96S02



Dual Retriggerable/Resetable Monostable Multivibrator

* DISCONTINUED

Diag. 274 16-Pin DIP See Fig. D8
ECG9615



Dual Differential Line Receiver